3A Rated µPOL™ DC-DC Converter with Integrated Inductor, Telemetry and Digital Power System Management

Features

- µPOL™ package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.35mm
- Continuous 3A load capability
- Plug and play: no external compensation required
- Programmable operation using the I^2C serial bus
- Voltage, current and temperature telemetry
- Operating temperature from -40°C to +125°C
- Wide input voltage range: 4.2V–16V
- Adjustable output voltage: 0.6V–5V
- ±0.5% initial output voltage accuracy
- Enable input with precise threshold
- Programmable under-voltage lock-out (UVLO)
- Open-drain power-good indicator
- Built-in protection features
- Servo loop for high-precision V_{OUT} regulation
- Offers eight I^2C addresses
- Lead-free and halogen-free

Applications

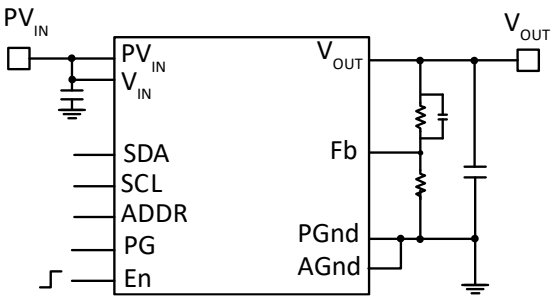
- Telecom and networking applications
- Data center applications
- 5G, AI applications
- Industrial applications
- Storage applications
- Distributed point-of-load power architectures

Description

The FS1003 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1003's operation using the Inter-Integrated Circuit (I^2C) protocol is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient, and fully featured 3A µPOL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.



Pin Configuration

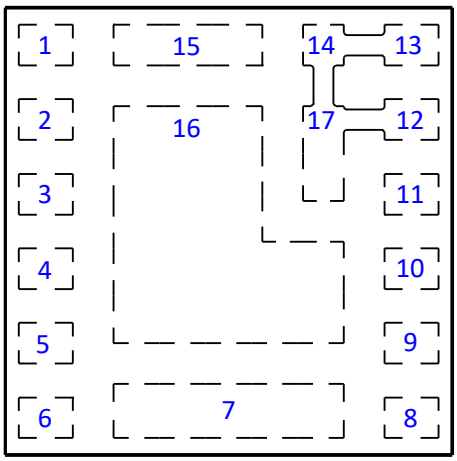


Figure 1 Pin layout (top view)

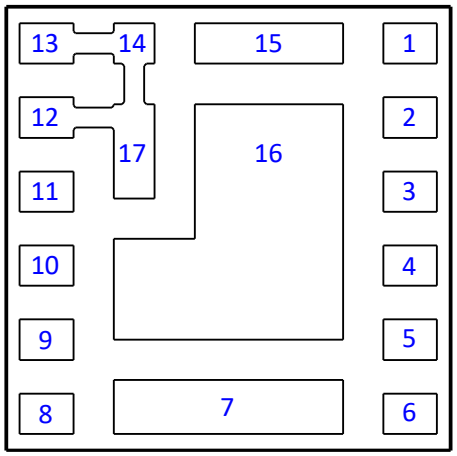


Figure 2 Pin layout (bottom view)

Pin Functions

Pin Number	Name	Description
1	SDA	**I²C Data Serial Input/Output line.** Pull up to bus voltage with a 4.99kΩ resistor. If unused, connect to AGnd.
2	PG	**Power Good status.** Open drain of an internal MOSFET. Pull up to V_{CC} (pin 10) or an external bias voltage, with a 49.9kΩ resistor
3	En	**Enable.** Switches the FS1003 on and off. Can be used with two external resistors to set an external UVLO (Figure 6).
4	SCL	**I²C Clock line.** Pull up to bus voltage with a 4.99kΩ resistor. If unused, tie to AGnd.
5	Fb	**Feedback.** Connect to V_{OUT} on the application board using an external resistor divider to set desired output voltage.
6	ADDR	**Address.** Connect to AGnd through a resistor to program FS1003 address (see 'I²C Base Address and Offsets' on page 16 and 'Switching Frequency and Minimum Values for On-time, Off-time and PV_{IN}' on page 16). May be shorted to AGnd or left open if I²C communication is not used.
7	V_{OUT}	**Regulator output voltage.** Place output capacitors between this pin and PGnd (pins 8 and 16).
8, 16	PGnd	**Power ground.** Serves as a separate ground for the MOSFETs. Connect to the power ground plane.
9	AGnd	**Signal ground.** Serves as the ground for the internal reference and control circuitry. Connect to pin 8 and also to the power ground plane through vias.
10	V_{CC}	**Supply voltage.** Output of the internal LDO regulator. It may also be used to apply an external V_{CC} voltage – when used in this way, connect V_{IN} to V_{CC}.
11	V_{IN}	**Input voltage.** Input for the internal LDO regulator. For single supply applications, connect to PV_{IN} using a 2.7Ω resistor. When using a separate V_{CC}, connect V_{IN} to V_{CC}.
12,13,14,17	PV_{IN}	**Power input voltage.** Input for the MOSFETs.
15	V_{SW}	**Test point for internal V_{SW}.** Connect to an isolated pad on the PCB.

Block Diagram

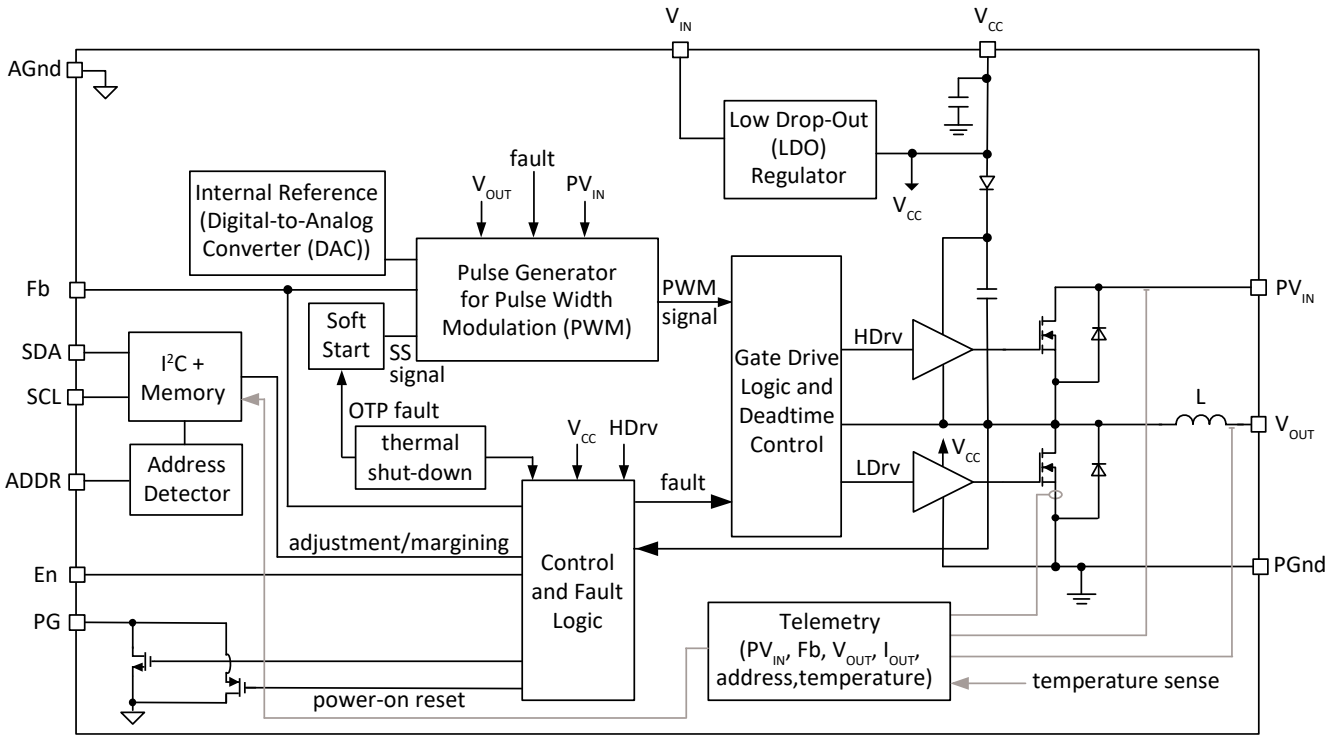


Figure 3 FS1003 µPOL™

Typical Applications

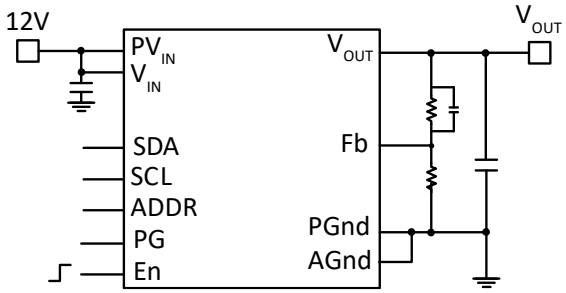


Figure 4 Single supply applications circuit

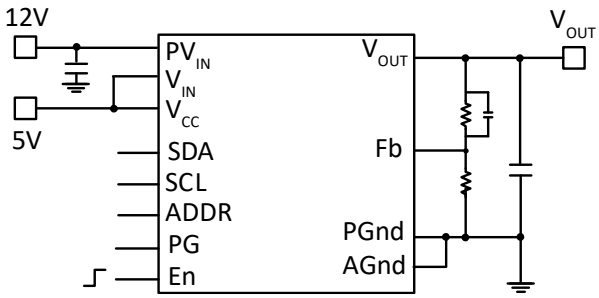


Figure 5 Dual supply applications circuit

Absolute Maximum Ratings

Warning: Stresses beyond those shown may cause permanent damage to the FS1003.

Note: Functional operation of the FS1003 is not implied under these or any other conditions beyond those stated in the FS1003 specification.

Reference	Range
PV_{IN}, V_{IN}, En to PGnd	-0.3V to 18V (Note 1, page 9)
V_{CC} to PGnd	-0.3V to 6V (Note 2, page 9)
Fb to AGnd	-0.3V to V_{CC} (Note 2, page 9)
PG to AGnd	-0.3V to V_{CC} (Note 2, page 9)
PGnd to AGnd	-0.3V to +0.3V
ESD Classification	2kV (HBM JESD22-A114)
Moisture Sensitivity Level	MSL 3 (JEDEC J-STD-020)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance Θ_{JA}	22.6°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}c\ (bottom)}$	2.36°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note: Θ_{JA} : FS1003 evaluation board and JEDEC specifications JESD 51-2A $\Theta_{J\text{-}c\ (bottom)}$: JEDEC specification JESD 51-8	

Order Information

Package Details

The FS1003 uses a µPOL™ 3.3 mm x 3.3 mm package delivered in tape-and-reel format (page 29). For more information on the tape-and-reel specification, go to:

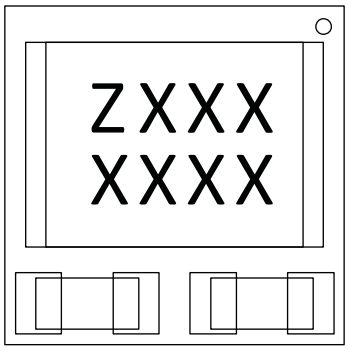
https://product.tdk.com/en/products/power/switching-power/micro-pol/designtool.html

Standard Part Number

Part Number	V_{OUT} (V)	Quantity per Reel	Package Description*	Package Designator
FS1003-0600-AL	0.60	3,000	17L Open Top LGA SiP	A01

* Compliant with EU Directives REACH and RoHS. RoHS is defined as semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances.

Package Markings



Z: V_{OUT}

XXXXXXX: Assembly Lot Code

FS1003	
Product	**Marking Code (Z)**
FS1003-0600	P

Recommended Operating Conditions

Definition	Symbol	Min	Max	Units
Input Voltage Range with External V_{CC} (Note 3, Note 5)	PV_{IN}	2.5	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	PV_{IN}, V_{IN}	4.5	16	
Supply Voltage Range (Note 2)	V_{CC}	4.5	5.5	
Output Voltage Range	V_O	0.6	5	
Continuous Output Current Range	I_O	0	3	A
Operating Junction Temperature	T_J	-40	125	°C

Electrical Characteristics

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} = V_{IN} < 16V, 0°C < T_J < 125°C **Typical values are specified at T_A = 25°C**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply Current						
V_{IN} Supply Current (Standby)	$I_{IN\ (STANDBY)}$	Enable low		2.1		mA
V_{IN} Supply Current (Static)	$I_{IN\ (STATIC)}$	No switching, En = 2V		3.7		
V_{IN} Supply Current (Dynamic)	$I_{IN\ (DYN)}$	En high, V_{IN} = PV_{IN} =12V, V_{OUT} = 0.6V, F_{SW} = 1.12MHz		14.5	18.6	
Soft-Start						
Soft-Start Rate	SS_{RATE} (default)	(Note 7)		0.5		V/ms
Output Voltage						
Output Voltage Range	V_{OUT} (default)			0.6		V
	V (resolution)			5		mV
Accuracy		T_J = 25°C, PV_{IN} = 12V, V_{OUT} = 0.6V (Note 6)	-0.5		0.5	%
		-40°C < T_J < 125°C (Note 6)	-1		1	
On-Time Timer Control						
On Time	T_{ON}	PV_{IN} = 12V, V_{OUT} = 0.6V, F_{SW} = 1.12MHz	39	46.5	55	ns
Minimum On-Time	$T_{ON(MIN)}$	(Note 7)		30		
Minimum Off-Time	$T_{OFF(MIN)}$	PV_{IN} = 0.6V		120	150	
Internal Low Drop-Out (LDO) Regulator						
LDO Regulator Output Voltage	V_{CC}	5.5V < V_{IN} = 16V, 0 – 20mA	4.9	5.2	5.5	V
		4.5V ≤ V_{IN} < 5.5V, 0 – 20mA	4.3			
Thermal Shut-Down						
Thermal Shut-Down	TSD (default)	(Note 7)		145		°C
Hysteresis				25		

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} = V_{IN} < 16V, 0°C < T_J < 125°C **Typical values are specified at T_A = 25°C**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Under-Voltage Lock-Out						
V_{CC} Start Threshold	V_{CC}_UVLO(START)	V_{CC} Rising Trip Level	3.95	4.15	4.35	V
V_{CC} Stop Threshold	V_{CC}_UVLO(STOP)	V_{CC} Falling Trip Level	3.6	3.8	3.95	
Enable Threshold	$En_{(HIGH)}$	Ramping Up	1.1	1.2	1.3	
	$En_{(LOW)}$	Ramping Down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Current Limit						
Current Limit Threshold	I_{OC} (default)	T_J = 25°C, PV_{IN} = 12V, V_{OUT} = 0.6V	3.6	4	4.3	A
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
Over-Voltage Protection						
Output Over-Voltage Protection Threshold	V_{OVP} (default)	OVP Detect (Note 7), V_{OUT} = 0.6V	115	120	125	Fb%
Output Over-voltage Protection Delay	T_{OVPDEL}			5		µs
Power Good (PG)						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	V_{OUT} Rising to 0.6V	86	90	95	Fb%
Power Good Hysteresis	$V_{PG(LOWER)}$	V_{OUT} Falling from 0.6V		5		
Power Good Sink Current	I_{PG}	PG = 0.5V, En = 2V		9		mA
Telemetry						
Input voltage reporting accuracy	PV_{IN}_report_pc	PV_{IN} = 12V, T_J = 25°C	-1.5		1.5	%
		5V < PV_{IN} < 16V, -40°C < T_J < 125°C (Note 6)	-1.5		1.5	%
Output voltage reporting accuracy	V_{OUT}_report_pc	V_{OUT} = V_{FB} = 0.6V, -40°C < T_J <125°C (Note 6)	-2		2	%
Output current reporting accuracy	I_{OUT}_report_acc	PV_{IN} = 12V, -40°C < T_J <125°C, V_{OUT} = V_{FB} = 0.6V, I_{OUT} = 0A (Note 6)	0		300	mA
Temperature reporting accuracy	T_report_acc	-40°C < T_J < 125°C (Note 7)	-10		10	°C

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
I^2C bus voltage	V_{BUS}		1.8	5.5	1.8	5.5	V
LOW-level input voltage	V_{IL}		−0.5	$0.3V_{BUS}$	−0.5	$0.3V_{BUS}$	
HIGH-level input voltage	V_{IH}		$0.7V_{BUS}$		$0.7V_{BUS}$		
Hysteresis	V_{HYS}		$0.05V_{BUS}$		$0.05V_{BUS}$		
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD} > 2 V,	0	0.4	0	0.4	
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current; V_{DD} ≤ 2 V,	0	$0.2V_{BUS}$	0	$0.2V_{BUS}$	
LOW-level output current	I_{OL}	V_{OL} = 0.4 V,	3	-	3	-	mA
		V_{OL} = 0.6 V	6	-	6	-	
Output fall time	T_{OF}	From V_{IHmin} to V_{ILmax}	20 × (V_{BUS}/5.5 V)	250	20 × (V_{BUS}/5.5 V)	125	ns
Pulse width of spikes that must be suppressed by the input filter	T_{SP}		0	50	0	50	
Input current each I/O pin	I_I		−10	10	−10	10	µA
Capacitance for each I/O pin	C_I		-	10	-	10	pF
SCL clock frequency	F_{SCL}		0	400	0	1000	kHz
Hold time (repeated) START condition	$T_{HD;STA}$	After this time, the first clock pulse is generated	0.6	-	0.26	-	µs
LOW period of the SCL clock	T_{LOW}		1.3	-	0.5	-	
HIGH period of the SCL clock	T_{HIGH}		0.6	-	0.26	-	
Set-up time for a repeated START condition	$T_{SU;STA}$		0.6	-	0.26	-	
Data hold time	$T_{HD;DAT}$	I^2C-bus devices	0	-	0	-	
Data set-up time	$T_{SU;DAT}$		100	-	50	-	ns
Rise time of SDA and SCL signals	T_R		20	300	-	120	
Fall time of SDA and SCL signals	T_F		20 × (V_{DD}/5.5 V)	300	20 × (V_{DD}/5.5 V)	120	
Set-up time for STOP condition	$T_{SU;STO}$		0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	T_{BUF}		1.3	-	0.5	-	
Capacitive load for each bus line	C_B		-	400	-	550	pF

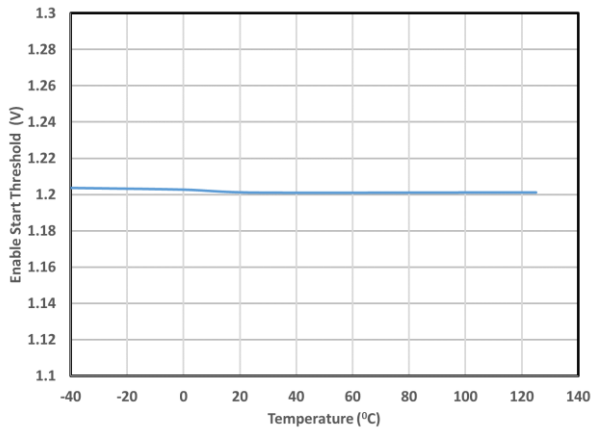
ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C **Typical values are specified at T_A = 25°C**							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
Data valid time	$T_{VD;DAT}$		-	0.9	-	0.45	µs
Data valid acknowledge time	$T_{VD;ACK}$		-	0.9	-	0.45	
Noise margin at the LOW level	V_{NL}	For each connected device, including hysteresis	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level	V_{NH}		$0.2V_{DD}$	-	$0.2V_{DD}$	-	
SDA timeout	T_{TO}		200		200		µs

Notes

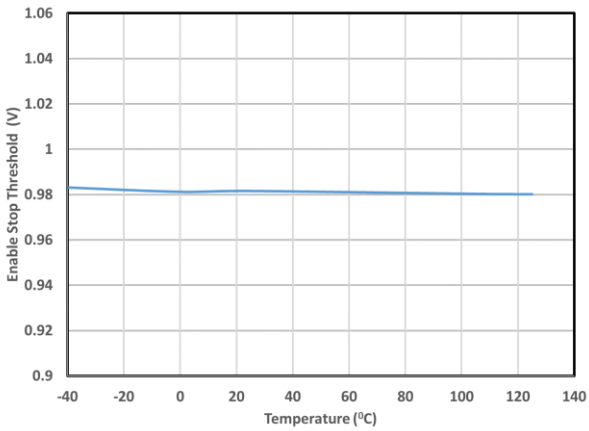
1 PGnd pin and AGnd pin are connected together
2 Must not exceed 6V
3 V_{IN} is connected to V_{CC} to bypass the internal Low Drop-Out (LDO) regulator
4 V_{IN} is connected to PV_{IN} (for single-rail applications with PV_{IN} = V_{IN} = 4.5V–16V)
5 Maximum switch node voltage should not exceed 22V
6 Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment
7 Guaranteed by design but not tested in production

Temperature Characteristics

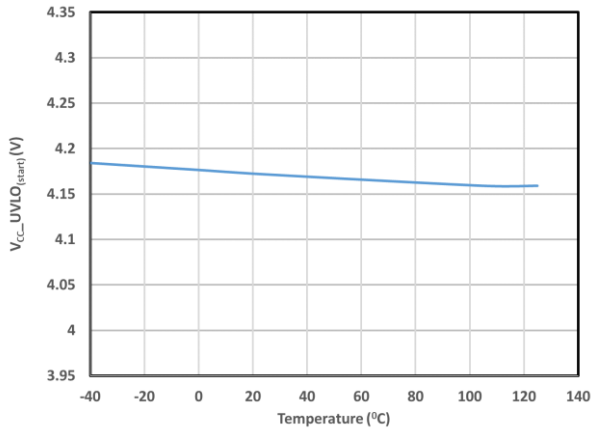
Enable Start Threshold



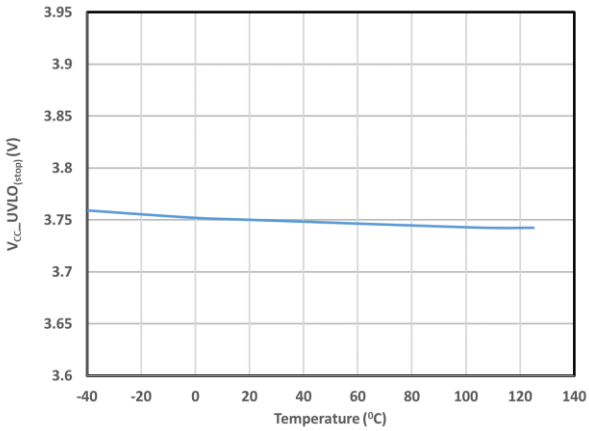
Enable Stop Threshold



V_{CC} Start Threshold

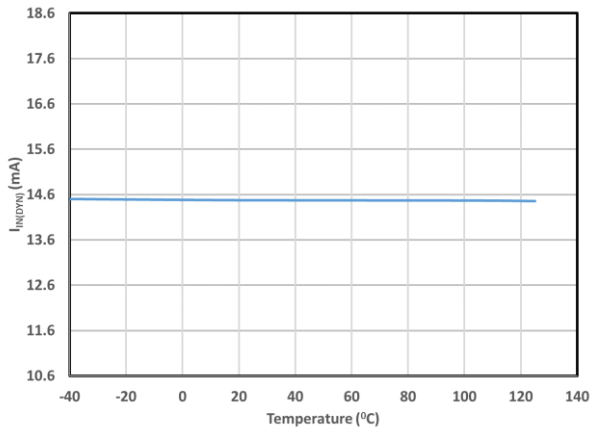


V_{CC} Stop Threshold

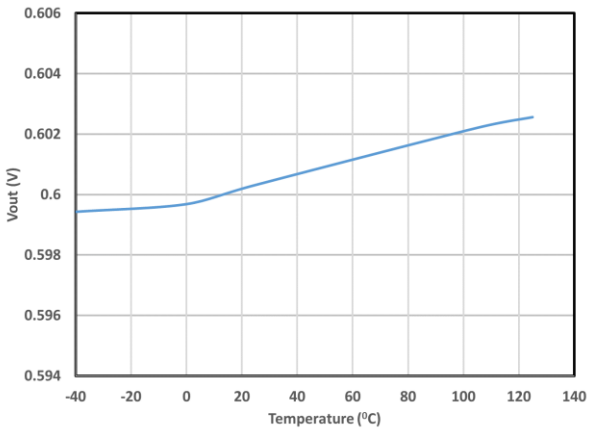


Temperature Characteristics

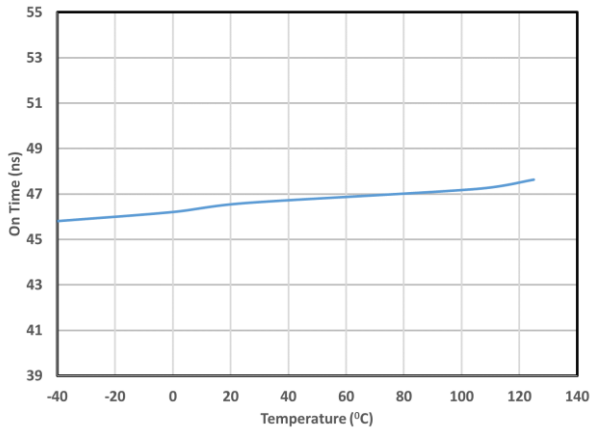
V_{IN} Supply Current (Dynamic)



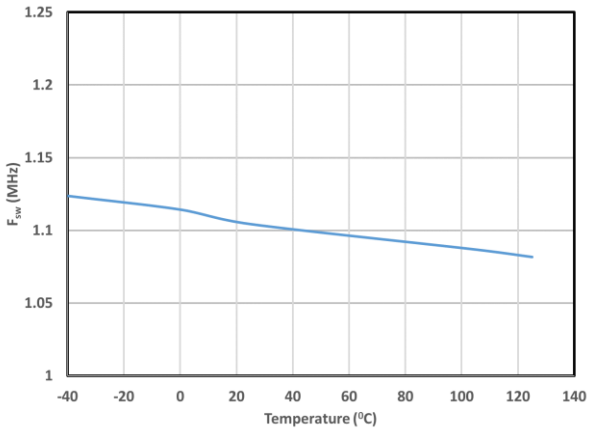
Output Voltage



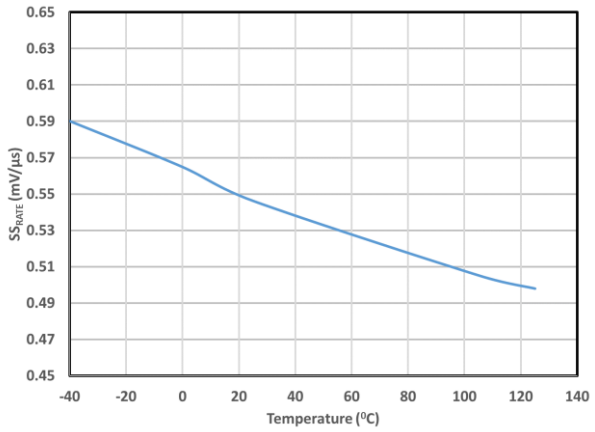
On Time



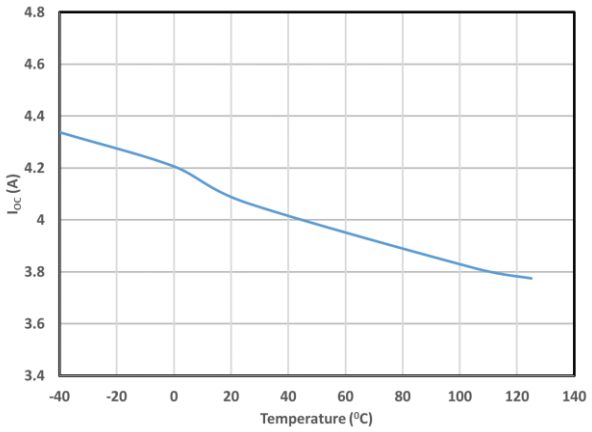
Switching Frequency



Soft-Start Rate



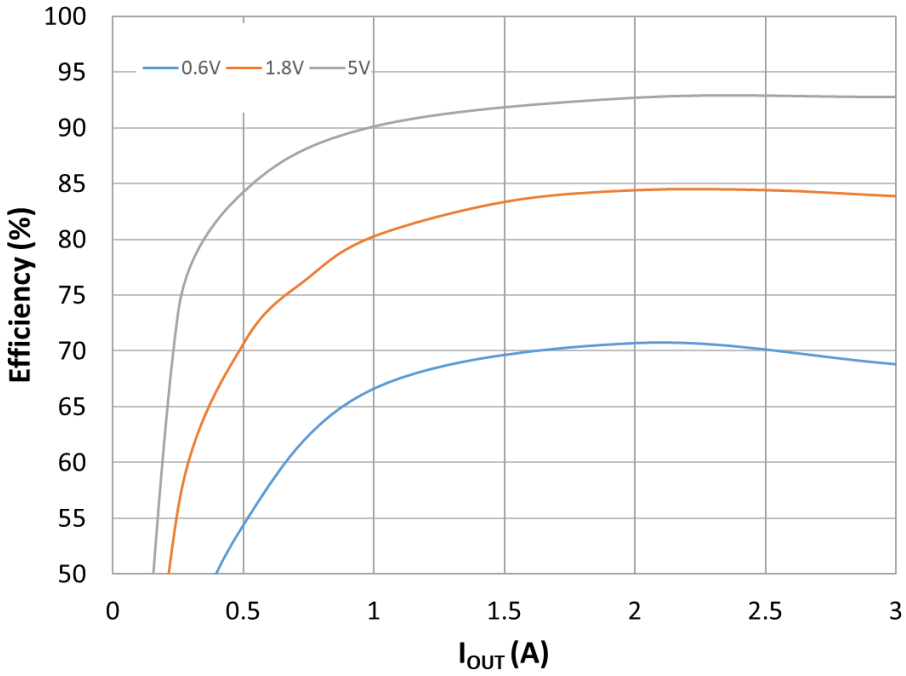
Current Limit Threshold

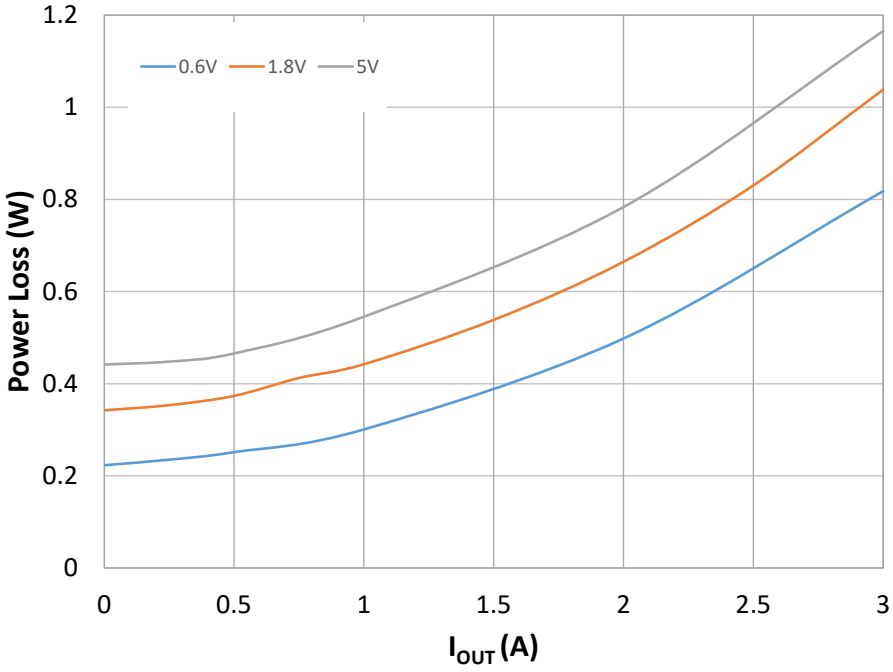


Efficiency Characteristics

Typical efficiency and power loss at PV_{IN} = 12V

PV_{IN} = 12V, Internal LDO used, I_{OUT} = 0A–3A, room temperature, no air flow, all losses included





Applications Information

Overview

The FS1003 is an easy-to-use, fully integrated, and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I²C protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues. An added servo loop ensures precise output voltage regulation.

Bias Voltage

The FS1003 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the V_{IN} pin should be connected to the PV_{IN} pin (Figure 6). If an external bias voltage is used, the V_{IN} pin should be connected to the V_{CC} pin to bypass the internal LDO regulator (Figure 7).

The supply voltage (internal or external) rises with V_{IN} and does not need to be enabled using the En pin. Consequently, I²C communication can begin as soon as:

- V_{CC}_UVLO start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

The I²C bus may be pulled up either to V_{CC} or to a system I²C bus voltage. The FS1003 offers two ranges for the I²C bus voltage, defined by the user register bit **Bus_voltage_sel**.

Register	Bits	Name/Description
0x1A	[1]	**Bus_voltage_sel** 0: 1.8–2.5V (default), 1: 3.3–5.0V

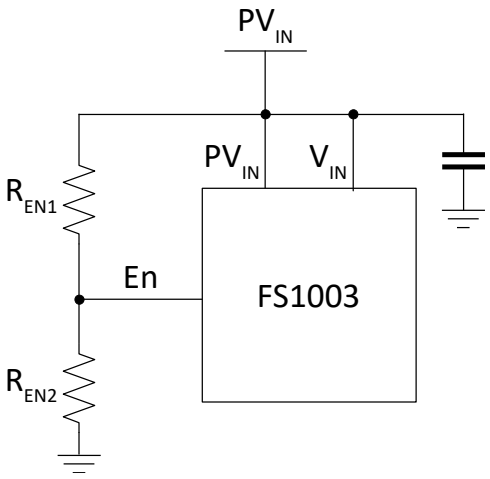


Figure 6 Single supply configuration: internal LDO regulator, adjustable PV_{IN}_UVLO

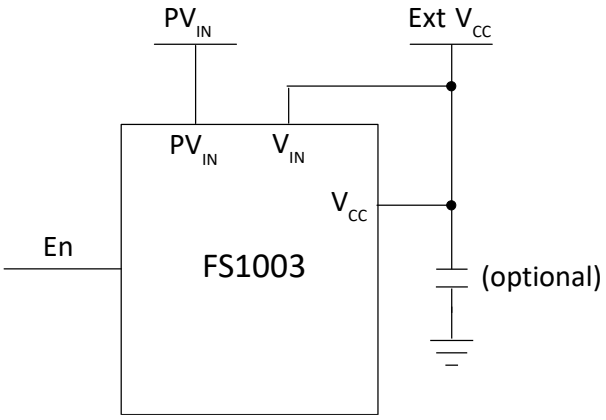


Figure 7 Using an external bias voltage

Soft-Start and Target Output Voltage

The FS1003 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When V_{CC} exceeds its start threshold (V_{CC}_UVLO$_{(START)}$), the FS1003 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset.

Once initialization is complete and the Enable (En) pin has been asserted (Figure 8), the internal reference soft-starts to the target output voltage at the rate defined by the user register bit **SS_rate**.

Register	Bits	Name/Description
0x14	[3]	**SS_rate** 0: 0.5mV/µs (default), 1: 1mV/µs

Note: When using FS1003-0600, even with a resistor divider, the rise time will always be 0.6V/SS_rate = 1.2ms (typical).

During initial start-up, the FS1003 operates with minimum-width high-drive (HDrv) pulses until the output voltage increases (see 'Switching Frequency and Minimum Values for On-time, Off-time and PV_{IN}' on page 16). On-time is increased until V_{OUT} reaches the target value defined by the user register bit **Vout_high_byte** and user register **Vout_low_byte**[7:0].

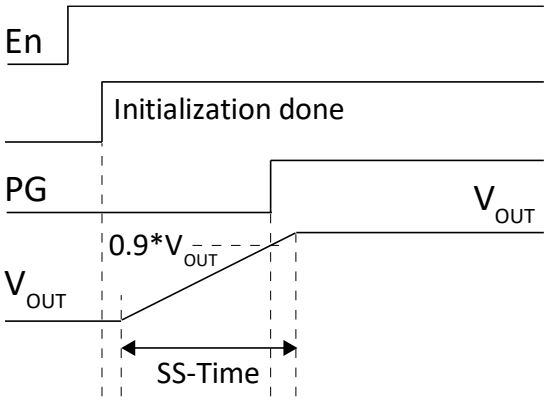


Figure 8 Theoretical operational waveforms during soft-start

Register	Bits	Name/Description
0x12	[0]	**Vout_high_byte**
0x13	[7:0]	**Vout_low_byte**

V_{OUT} is set in increments of 5mV and may be used to adjust the output voltage up to ±20%. Use the following equation to calculate the V_{OUT} code to enter into **Vout_high_byte** and **Vout_low_byte**[7:0]:

$$Vout_{code} = \frac{Vout_{target} - 0.4}{0.005}$$

All voltages and resolutions are in Volts.

For example:

To set V_{OUT} = 0.625V:

$$Vout_{code} = \frac{0.625 - 0.4}{0.005} = 45$$

45 is 02D in hexadecimal, therefore:

Set **Vout_high_byte** to 0

Set **Vout_low_byte** to 2D or $(101101)_b$

Over-current protection (OCP) and over-voltage protection (OVP) is enabled during soft-start to protect the FS1003 from short circuits and excess voltages respectively.

The output voltage may be set using a resistor divider to the feedback pin (Figure 9). This gives system designers the flexibility to design all the power rails in the system across the output voltage range from 0.6V to 5V using a single part.

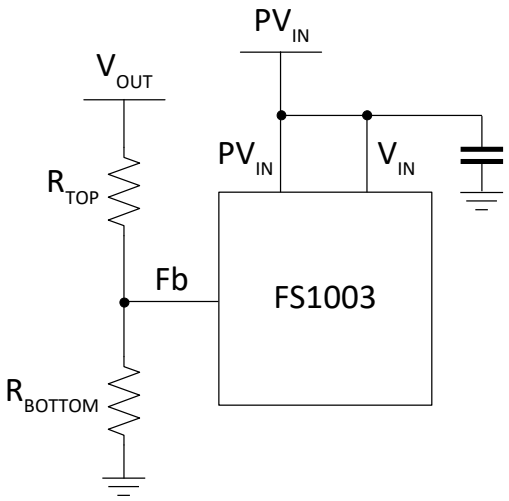


Figure 9 Setting the output voltage with an external resistor divider

The equation below describes the appropriate resistor divider selection to set the output voltage using a FS1003 programmed to 0.6V.

$$\frac{R_{TOP}}{R_{BOTTOM}} = 1.667V_{OUT} - 1 - 0.0000066R_{TOP}$$

It is recommended that system designers place a capacitor of 47pF to 680pF in parallel with R_{TOP}, for which a value of 4.12kΩ is recommended. The recommended value for R_{BOTTOM} (using standard 1% resistor values) depends on the output voltage, as shown in Table 1.

Table 1 Recommended resistance values

V_{OUT} (V)	R_{TOP} /R_{BOTTOM}	V_{OUT} (V)	R_{TOP} /R_{BOTTOM}
0.65	0.0563	1.10	0.8063
0.70	0.1401	1.18	0.9321
0.72	0.1738	1.20	0.9763
0.80	0.3098	1.50	1.4714
0.85	0.3924	1.80	1.9619
0.90	0.4758	2.50	3.1692
0.95	0.5628	3.0	3.9238
1.00	0.6348	3.3	4.4253
1.05	0.7331	5.0	7.3309

Pre-biased Start-up

The FS1003 can start up into a pre-charged output smoothly, without causing oscillations and disturbances of the output voltage. When it starts up in this way, the Control and Synchronous MOSFETs are forced off until the internal Soft-Start (SS) signal exceeds the sensed output voltage at the Fb pin. Only then is the first gate signal of the Control MOSFET generated, followed by complementary turn on of the Synchronous MOSFET. The Power Good (PG) function is not active until this point.

Shut-down Mechanisms

The FS1003 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*
  Initiated by de-asserting the En pin. Both drivers switch off and the digital-to-analog converter (DAC) and soft-start are pulled down instantaneously.

- *Soft-Stop or controlled ramp down*
  Initiated by setting user register bit **SoftStopEnable** to 1 ***and*** user register bit **SoftDisable** to 1. The SS signal falls to 0 at the same rate as it rises during start-up; the drivers are disabled only when it reaches 0. The output voltage then follows the SS signal down to 0.

  The **SoftDisable** bit must not be toggled while the part is enabled and switching. Instead, for applications requiring soft-stop, this bit must be set to 1 and, with the En pin asserted, the **SoftStopEnable** bit must be toggled to soft-start or soft-stop the device.

  By default, both the **SoftDisable** bit and the **SoftStopEnable** bit are 0, which means that soft-stop operation is disabled by default.

Register	Bits	Name/Description
0x14	[2]	**SoftStopEnable**
0x1C	[3]	**SoftDisable**

I²C Base Address and Offsets

The FS1003 has a user register called **Base_address**[7:0] stored in memory that sets its base I²C address. The default base address is 0x08. An offset of 0 to 7 is then defined by connecting the ADDR pin to the AGnd pin either directly or through a resistor (1% or better). An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I²C address to set the address at which the I²C master device will communicate with the FS1003.

To select offsets of 0 to 7, connect the pins as shown in Table 2.

Table 2 Address Offset Resistance Values

Resistor (kΩ)	Addr Offset
0.00*	**0**
1.13	**+1**
1.87	**+2**
2.61	**+3**
3.40	**+4**
4.12	**+5**
4.87	**+6**
5.62	**+7**
* Short ADDR to AGnd.	

Note: When using the FS1003, I²C addresses (7-bit addressing) 0x48 to 0x4F are unavailable and should not be used.

Switching Frequency and Minimum Values for On-time, Off-time and PV_{IN}

The switching frequency of the FS1003 depends on the output voltage.

The frequency at which the device will switch changes automatically depending on the output voltage set by the feedback resistor divider. Table 3 shows nominal switching frequencies for various output voltages, with an input voltage of 12V.

Table 3 Switching Frequencies (adjustable V_{OUT})

V_{OUT} (V)	F_{SW} (MHz)
0.6	0.9
0.8	1.23
1.0	1.33
1.1	1.36
1.2	1.39
1.5	1.47
1.8	1.51
2.5	1.58

For output voltages of 0.8V and above, select the address resistor as shown in Table 2. For output voltages lower than 0.8V, and also for output voltages above 3.3V when the input voltage is below 7V, select the address resistor as shown in Table 4.

The ADDR pin serves a dual function: to set up to seven address offsets and, at the same time, allow the switching frequency to be adjusted by 300kHz. For example, for 5V output, an address resistor value of 4.87kΩ sets the address offset to +6 and the switching frequency to 1.65MHz; an address resistor value of 11kΩ sets the same address offset (+6) but sets the switching frequency to 1.35MHz.

Table 4 Switching Frequency Resistance Values

Resistor (kΩ)	Addr Offset
6.34	**0**
7.15	**+1**
7.87	**+2**
8.66	**+3**
9.42	**+4**
10.20	**+5**
11.00*	**+6**
12.10	**+7**
* If T_J < 20°C, use a 10.9kΩ ±0.5% resistor.	

When input voltage is high relative to target output voltage, the Control MOSFET is switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$), nominally 30ns. During start-up, when the output voltage is very small, the FS1003 operates with minimum on-time.

When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ($T_{OFF(MIN)}$), nominally 120ns. The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

Enable (En) Pin

The Enable (En) pin has several functions:

- It is used to switch the FS1003 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1003 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the PV_{IN} voltage by a set of resistive dividers, R_{EN1} and R_{EN2} (Figure 6). Users can program the UVLO threshold voltage by selecting different ratios. This is a useful feature that stops the FS1003 regulating when PV_{IN} is lower than the desired voltage.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 10).

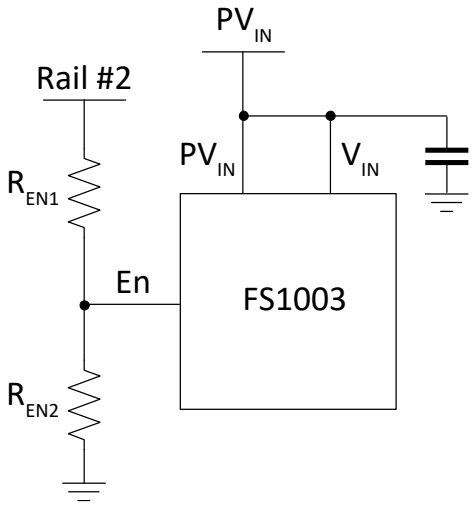


Figure 10 En pin used to monitor other rails for sequencing purposes

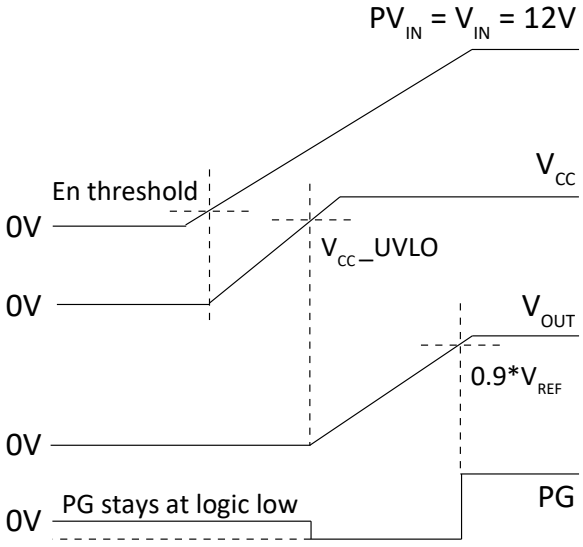


Figure 11 Start-up: PV_{IN}, V_{IN} tied together, En connected to resistor divider from PV_{IN} PG pin pulled up to an external supply

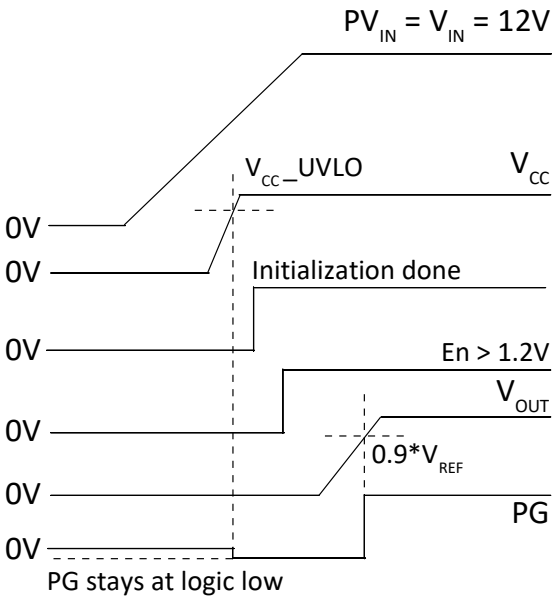


Figure 12 Start-up: En pin asserted after PV_{IN} and V_{IN}, PG pin pulled up to an external supply

For V_{OUT} to start up as defined by the soft-start rate requires correct sequencing:

- PV_{IN} must start up before V_{CC} and/or Enable.
- PV_{IN} must ramp down only after V_{CC} has ramped down below its UVLO threshold and/or Enable has been de-asserted.

Over-current Protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is defined by the user register bits **OCSet**.

Register	Bits	Name/Description
0x15	[2:0]	**OCSet** 0: 4A

The threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1003 enters hiccup mode (Figure 13). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1003 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1003 remains in hiccup mode until the over-current fault is remedied.

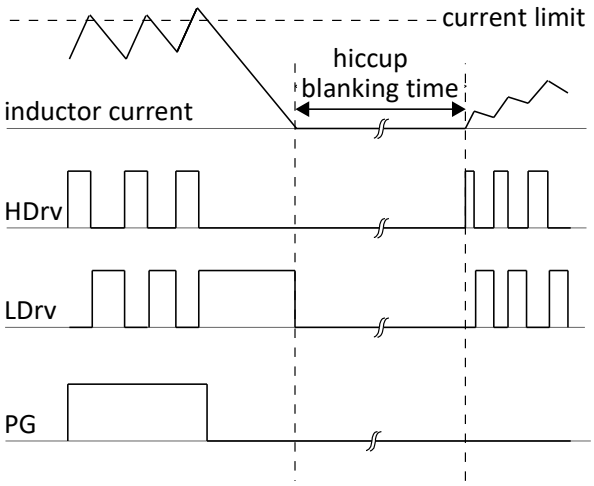


Figure 13 Illustration of OCP in hiccup mode

Over-voltage Protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the Fb pin. When Fb exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is defined by the user register bits **OV_Threshold**.

Register	Bits	Name/Description
0x17	[1:0]	**OV_Threshold** 0:105% of V_{OUT} 1:110% of V_{OUT} 2:115% of V_{OUT} 3:120% of V_{OUT} (default)

The Control MOSFET is switched off immediately and the PG pin is pulled low. The Synchronous MOSFET is switched on to discharge the output capacitor.

The Control MOSFET remains latched off until reset by cycling either V_{CC} or En. The voltage at the Fb pin falling below the output OVP threshold (with 5% hysteresis) does not switch on the Control MOSFET but it does switch off the Synchronous MOSFET to prevent build-up of negative current.

Figure 14 shows a timing diagram for over-voltage protection.

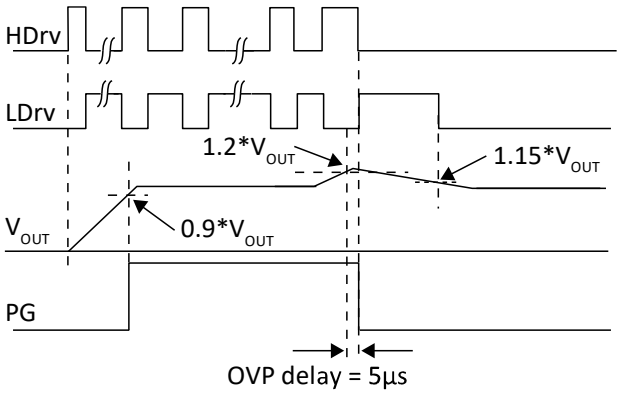


Figure 14 Illustration of latched OVP

Over-temperature Protection (OTP)

Temperature sensing is provided inside the FS1003. The OTP threshold is defined by the user register bits **OT_Threshold**.

Register	Bits	Name/Description
0x19	[1:0]	**OT_Threshold** 0:75°C 1: 85°C 2: 125°C 3: 145°C (default)

When the threshold is exceeded, thermal shut-down switches off both MOSFETs and resets the internal soft-start, but the internal LDO regulator is still in operation.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

Telemetry (ADC)

FS1003 has telemetry through I^2C. Parameters PV_{IN}, V_{OUT}, Fb, I_{OUT} and temperature can be read through the telemetry.

Telemetry	Resolution	Min	Max
V_{IN} (V)	1/16	0	15.9375
V_{OUT} (V)	0.01	0.6	2.5
Fb (V)	0.01	0.6	0.6
I_{OUT} (A)	0.03125	0	3
Temperature (°C)	1	-40	145

PV_{IN} reporting is calculated by dividing the decimal equivalent of the contents of register 0x0C by 16. V_{OUT} is calculated from the contents of register 0x0D: multiplying the decimal equivalent by 10mV and then adding 300mV to it. For output voltages higher than 2.85V, the Fb voltage reading should be used and scaled by target V_{OUT}/0.6. The Fb voltage is calculated from the contents of register 0x22, multiplying the decimal equivalent by 10mV and then adding 300mV to it. Finally, register 0x0F reports the temperature in 1°C resolution.

For current reporting, the contents of register 0x0E are read and converted to decimal (*iout_report_dec*). Then register 0x1A is read and **Reg_0x1A**[7:2] is converted to decimal (*G_dec*).

For FS1003:

$$i_{report\_calc} = \frac{i_{out\_report\_dec}}{32} - (4.4221 - 0.1184 \times G_{dec}) \times V_{OUT} - 0.5164 \times G\_dec + 18.71$$

Servo Loop and Precision Output Voltage

FS1003 has an internal servo loop to minimize V_{OUT} error at steady state. Load and line regulation of better than ±1% is achieved.

Power Good (PG)

Power Good (PG) behavior is defined by the user register bits **PGControl** and **PG_Threshold**.

Register	Bits	Name/Description
0x18	[1:0]	**PG_Threshold** 0:80% of V_{OUT} 1: 85% of V_{OUT} 2: 90% of V_{OUT} (default) 3: 95% of V_{OUT}
0x14	[0]	**PG_Control** 1:Threshold based (default) 0: DAC based

PG_Threshold Bit

The user register bit **PG_Threshold** defines the PG threshold as a percentage of V_{OUT}. Hysteresis of 5% is applied to this, giving a lower threshold.

When Fb rises above the upper threshold, the PG signal is pulled high. When Fb drops below the lower threshold, the PG signal is pulled low.

PGControl Bit Set to 1 (default)

Figure 15 shows PG behavior in this situation.

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- En and V_{CC} are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- V_{OUT} is within the target range (determined by continuously monitoring whether Fb is above the PG threshold)

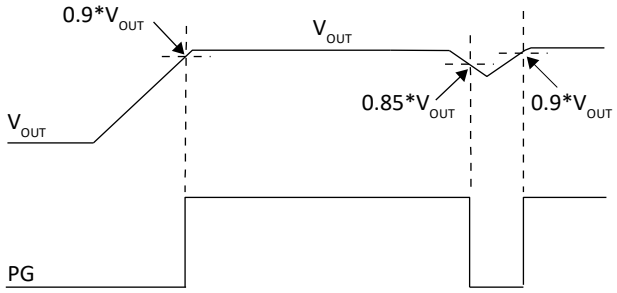


Figure 15 PG signal when PGControl bit=1

PGControl Bit Set to 0

Figure 16 shows PG behavior in this situation.

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after soft-start is within 2% of target output voltage, not when Fb exceeds the upper PG threshold.

For pre-biased start-up, the PG signal is not active until the first gate signal of the Control MOSFET is generated.

FS1003 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if V_{CC} is low and the PG pin is pulled up to an external voltage not V_{CC} (Figure 11 and Figure 12).

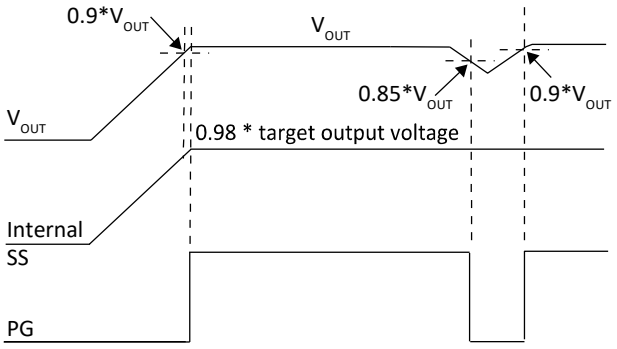


Figure 16 PG signal when PGControl bit=0

Design Example

Let us now consider a simple design example, using the FS1003 for the following design parameters:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 1.8V$
- $F_{SW} = 1.5MHz$
- $C_{OUT} = 2 \times 22\mu F$
- $C_{IN} = 2 \times 22\mu F$
- Ripple Voltage = ± 1% * V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% * V_{OUT}
  (for 50% load transient)

Input Capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1003.
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple.

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For a buck converter operating at duty cycle D and output current I_O, the RMS value of the input current is:

$$I_{RMS} = Io\sqrt{D(1-D)}$$

In this application, I_O = 3A and $D = \frac{V_{OUT}}{PV_{IN}} = 0.15$

Therefore, I_{RMS} = 1.07A and we can select two 22µF 16V ceramic capacitors for the input capacitors (C2012X5R1C226K125AC from TDK).

If the FS1003 is not located close to the 12V power supply, a bulk capacitor (68–330µF) may be used in addition to the ceramic capacitors.

For V_{IN}, which is the input to the LDO, it is recommended to use a 1µF capacitor very close to the pin. The V_{IN} pin should be connected to PV_{IN} through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1µF capacitor filter noise on PV_{IN}.

Output Voltage and Output Capacitor

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1003, the minimum number of output capacitors required to achieve target peak-to-peak V_{OUT} ripple is:

$$N_{MIN} = 1.2 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- N_{MIN} = minimum number of output capacitors
- D = duty cycle
- C = equivalent capacitance of each output capacitor
- F_{SW} = switching frequency
- ESR = equivalent series resistance of each output capacitor
- ESL = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$
  = target peak-to-peak V_{OUT} ripple

This design uses C2012X5R0J226K125AB from TDK; this is a 22µF MLCC, 0805 case size, rated at 6.3V. At 1.8V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 12µF (C). Equivalent series resistance is 3mΩ (ESR) and equivalent series inductance is 0.44nH (ESL).

Putting these parameters into the equation gives:

N_{MIN} = 0.39

To meet the maximum voltage deviation ΔV_{OUTmax} under a ΔI_o load transient, the minimum required number of output capacitors is:

$$\frac{500 \times 10^{-9} \times \Delta I_o^2}{\Delta V_{OUTmax} \times F_{sw} \times C}$$

where:

- ΔI_o = load step
- ΔV_{OUTmax} = target maximum voltage deviation

- F_{sw} = switching frequency
- C = equivalent capacitance of each output capacitor

Again, using C = 12µF, it can be seen that the minimum number of output capacitors required is 0.96.

In our design intended for space-constrained applications, we use two C2012X5R0J226K125AB capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

a) No ESR or ESL

b) Converter can saturate its duty cycle instantly.

c) No latency

d) Step load (infinite slew rate)

Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

It should be noted that even in the absence of a target V_{OUT} ripple or target maximum voltage deviation under load transient, at least one 22µF capacitor is still required to ensure stable operation without excessive jitter.

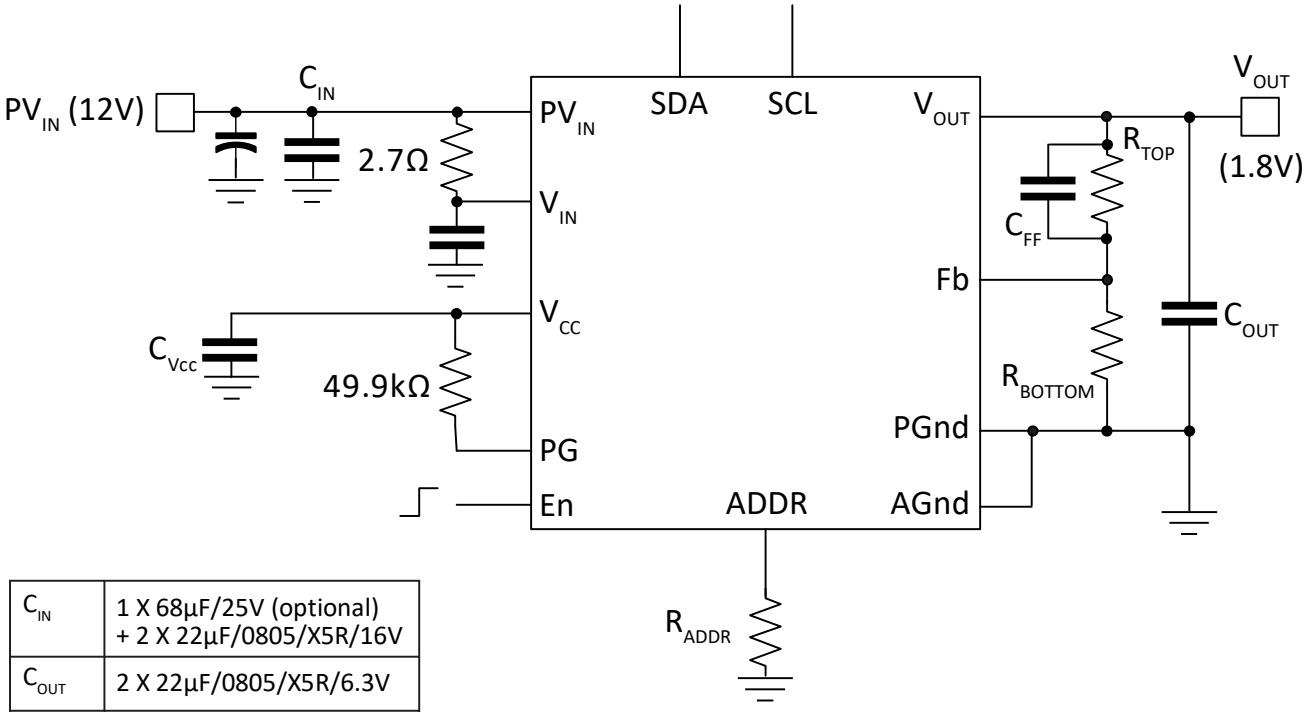
Up to six 22µF capacitors may be used in the design. If more capacitance is required, it is recommended to use a capacitor with relatively high ESR (>3mΩ), such as POSCAP or specialty polymer capacitors.

Resistor Divider Selection

The recommended top resistor value (R_{TOP}) is 4.12kΩ, while the bottom resistor value (R_{BOTTOM}) depends on the required output voltage (see Table 1 on page 15). When using an FS1003-0600 to generate 1.8V, the table gives a ratio of 1.9619: this results in a value of 2.1kΩ for R_{BOTTOM}. A feed-forward capacitor C_{FF} = 680pF is used in parallel with R_{TOP}; this allows greater flexibility in choice of output capacitance.

V_{CC} Capacitor Selection

FS1003 uses an on-package V_{CC} capacitor to ensure effective high-frequency bypassing. However, especially for applications that use an external V_{CC} supply, it is recommended that system designers place a 2.2µF/0603/X7R/10V capacitor on the application board as close as possible to the V_{CC} pin.



C_{IN}	1 X 68µF/25V (optional) + 2 X 22µF/0805/X5R/16V
C_{OUT}	2 X 22µF/0805/X5R/6.3V
C_{Vcc}	2.2µF/0603/X5R/10V
R_{TOP}	4.12kΩ
R_{BOTTOM}	2.10kΩ
C_{FF}	680pF

Note: For values of R_{ADDR}, see Table 2 and Table 4 on page 16

Figure 17 Application circuit for a single supply, PV_{IN} = 12V, V_{OUT} = 1.8V, 3A

Layout Recommendations

FS1003 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the V_{CC} bypass capacitor (if used), should be placed as close as possible to the FS1003 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Through-hole vias should be used to connect the analog ground to the power ground plane.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not covered with solder mask. Via In Pad Plated Over (VIPPO) techniques are acceptable.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.
- SCL and SDA traces must be at least 10mil wide, with 20–30mil spacing between them.

Thermal Considerations

The FS1003 has been thermally tested and modeled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1003 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

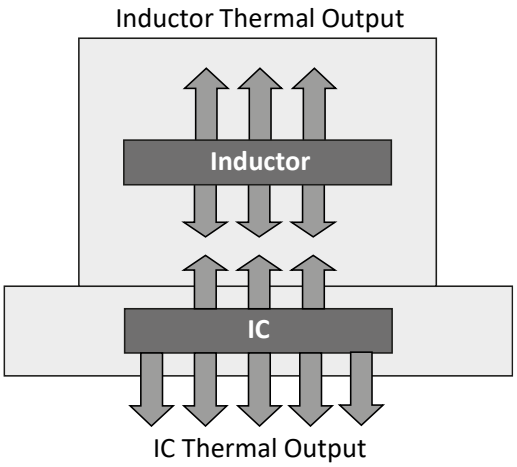


Figure 18 Heat sources in the FS1003

Figure 19 shows the thermal resistances in the FS1003, where:

- Θ_{JA} is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$ is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- Θ_{JCtop} is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1003 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

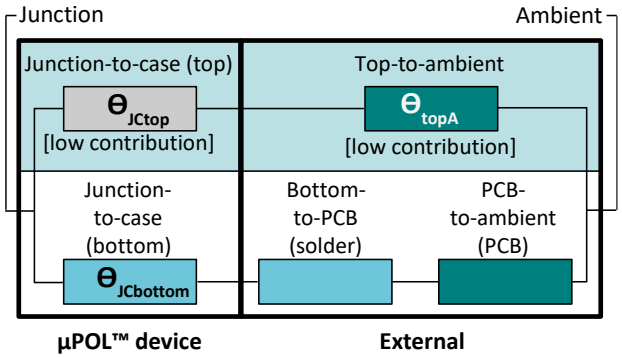


Figure 19 Thermal resistances of the FS1003

The values of the thermal resistances are:

- Θ_{JA} = 22.6°C/W
- $\Theta_{JCbottom}$ = 2.36°C/W

Although these values indicate how the FS1003 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the µPOL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

I²C Protocol

S	=	Start bit	W	=	Write bit (‘0’)	White bits	=	Issued by master
P	=	Stop bit	R	=	Read (‘1’)	Grey bits	=	Sent by slave (FS1003)
A	=	Ack	Sr	=	Repeated start			
N	=	Nack						

Write transaction

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Register Address	A	Data Byte	A	P

Read transaction

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data Byte	N	P

Package Description

The FS1003 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate.

As a result of these properties, the FS1003 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's µPOL™ package series P11F1, including important guidance on checking the compatibility of manufacturing processes such as cleanable flux systems.

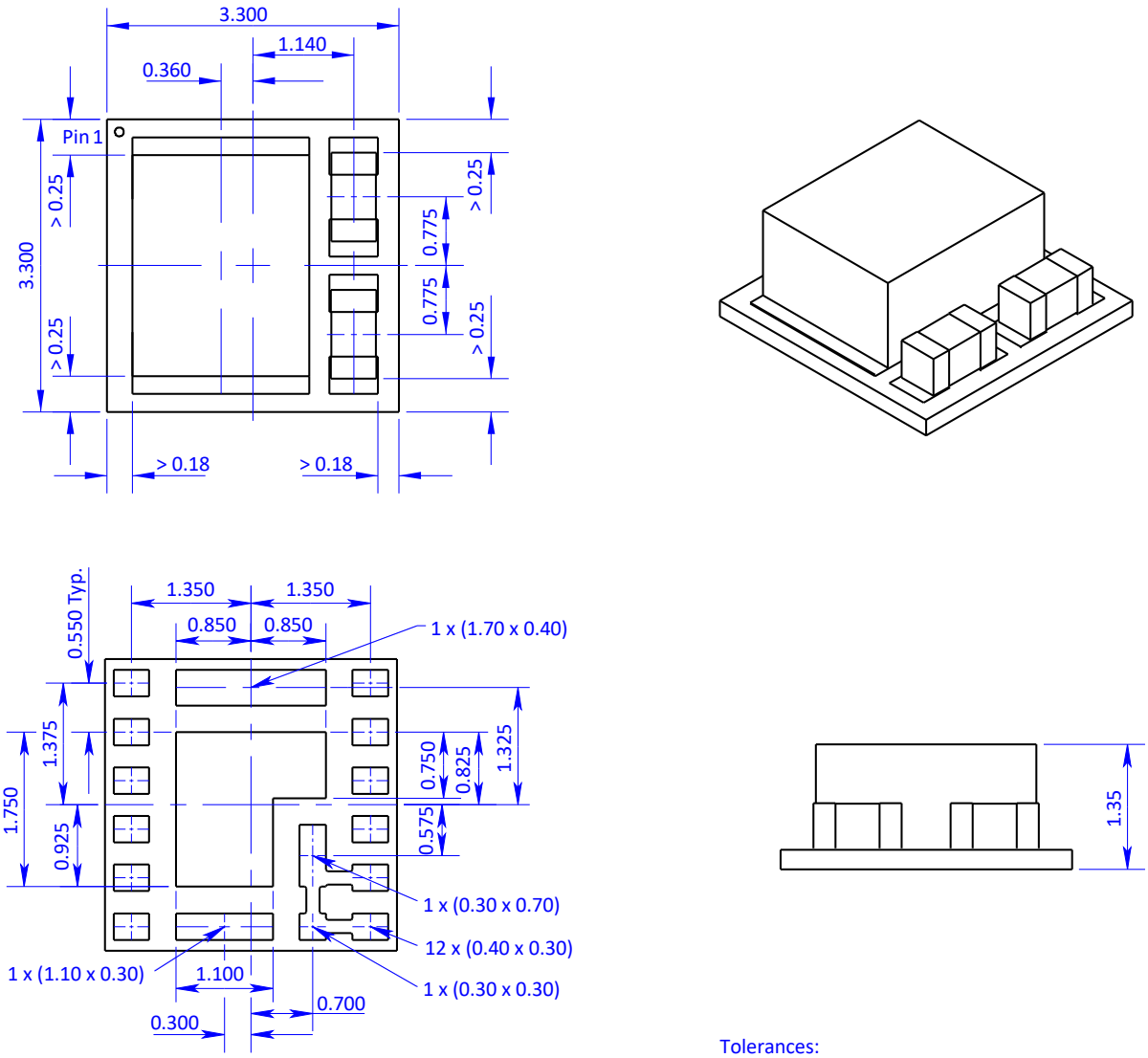
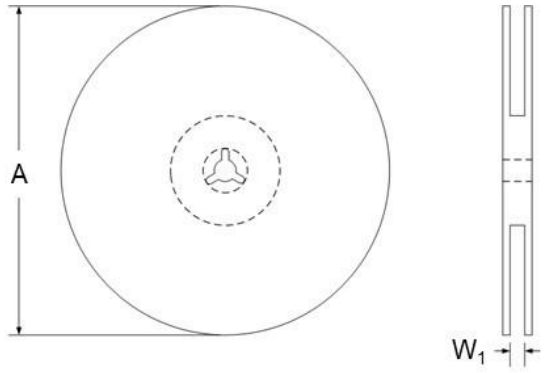


Figure 20 Dimensioned drawings

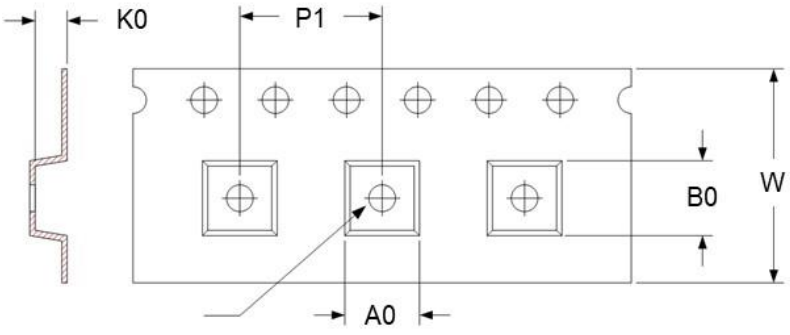
Tape and Reel Information

Reel Dimensions



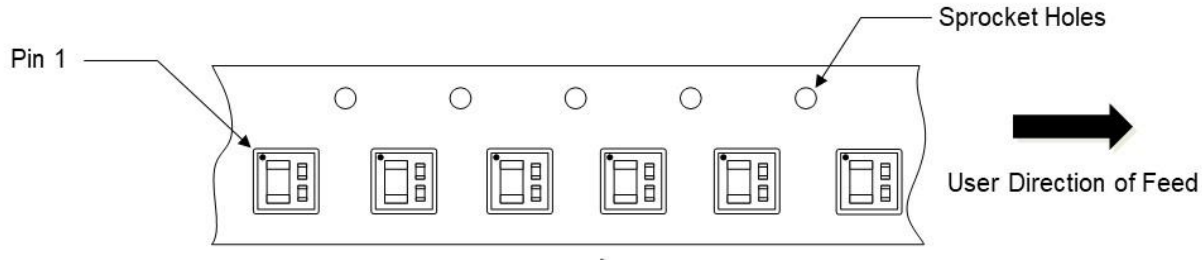
Reel Diameter A (mm)	Reel Width W_1 (mm)
330	12.8

Tape Dimensions



Dimension	(mm)
P1	8.0
W	12.0
A0	3.6
B0	3.6
K0	1.8

Pin 1 Orientation in Carrier Tape



REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

REMINDER

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety. To allow flexibility in the applications of the FS100x device family, some parameters are accessible to the users through an I^2C/PMBus™ interface. These parameters can only be changed within limits that are acceptable to the device. However, it is the responsibility of the user to ensure that any parameter change, whether it be deliberate or inadvertent, does not violate the specifications of the end user system.