**Target Specification**

**25A Stackable µPOL™** Regulator with Integrated Inductor and Digital Power System Management

# Features

- µPOL™ package with output inductor included
- Small size: **6.80mm x 7.65mm x 3.75mm**
- Continuous 25A load capability
- Stackable up to **200A** (8 Modules)
- Plug and play: no external compensation required
- True Differential Remote Sensing
- Programmable operation using I²C and PMBus™
- Wide input voltage range: 4.5V–16V
- Adjustable output voltage upto 1.8V
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good indicator
- Built-in protection features
- Operating temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU Directives REACH and RoHS 6

# Applications

- Telecom and networking applications
- Data Center applications
- Storage applications
- Industrial applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation

# Description

The FS1525 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1525's operation using the I²C and PMBus™ protocols is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient and fully featured **25A – 200A µPOL™** currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.
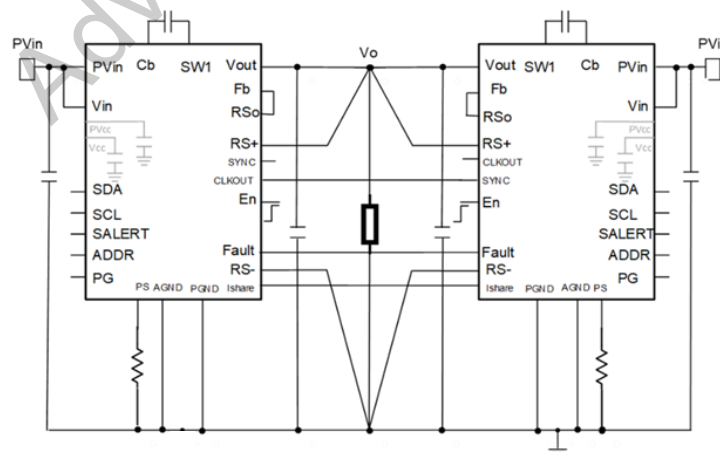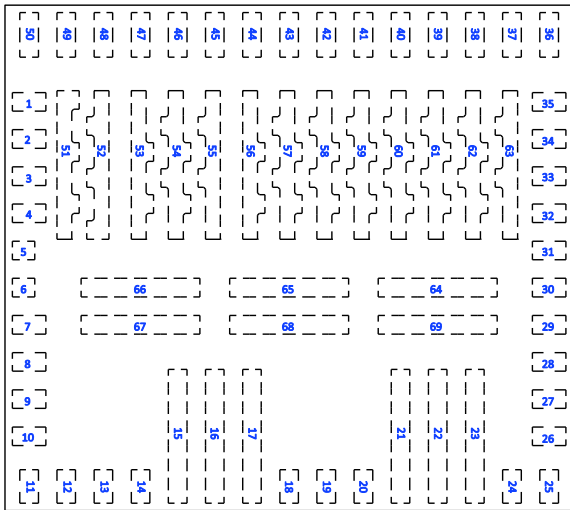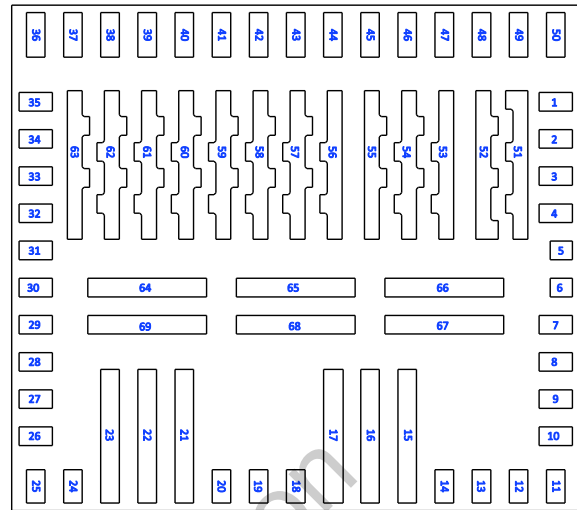
*Figure 1    Pin layout (top view)*



*Figure 2    Pin layout (bottom view)*

## Pin functions

| Pin Numbers | Pin Name | Pin Description |
|---|---|---|
| 44 | NC | Test pin for Sync FET of phase 2 |
| 8 | Vin | Input supply to the internal LDO. Connect to PVin through a 2.7 ohm resistor |
| 25 | En | Enable pin to turn the device ON & OFF.  It can be used to set an external UVLO by using two external resistors |
| 9 | PVcc | Input supply for the drivers. Connect to Vcc on the application board. |
| 10 | Vcc | Input bias for an external VCC voltage / Output of the internal LDO. |
| 13 | VFB | Feedback voltage to the device. Connect to Vout on the application board if remote sense is not used, or to Rso if remote sense is used. |
| 64-69 | AGnd | Signal ground for the internal reference and control circuitry. |
| 21, 22, 23 | VOUT1 | Power output from regulator. VOUT1 and VOUT2 should be shorted by VOUT plane on PCB. Place output capacitors between Vout & PGND |
| 15, 16, 17 | VOUT2 | Power output from regulator. VOUT1 and VOUT2 should be shorted by VOUT plane on PCB. Place output capacitors between Vout & PGND |
| 30 | PGOOD | Power Good status pin. Output is an open drain. Connect a pull up resistor between this pin & VCC or to an external bias voltage. |

| 12 | ADDR | Program Device address by connecting a resistor from this pin to ground; up to 16 address offsets may be programmed |
|---|---|---|
| 5 | Boot1 | Boot pin for phase 1 driver |
| 6 | Boot2 | Boot pin for phase 2 driver |
| 7 | SYNC | Pin to synchronize device with external clock. |
| 29 | Clkout | Phase shifted clock out. Connect to sync of next slave in daisy chain |
| 27 | SDA | I2C/PMBus Data Serial Input/Output line.  Pull up to bus voltage with 4.99K resistor |
| 26 | SCL | I2C/PMBus Clock line. Pull up to bus voltage with 4.99K resistor |
| 28 | ALERT | SMBAlert# line.  Pull up to bus voltage with 4.99K resistor. |
| 36-43 | SW1 | Drain of Sync FET of phase 1. An external fly cap may be connected between this pin and Cb |
| 31-35, 56-63 | PGnd | Power Ground. This pin serves as a separate ground for the MOSFETs and should be connected to the system's power ground plane. |
| 45-50, 53, 54, 55 | Cb | Connection for an external cap. The capacitor connects between this pin and VSW1 and should be connected as close as possible to these pins |
| 18 | RS+ | Input of differential remote sense amplifier. Connect to Vo |
| 19 | RS- | Input of differential remote sense amplifier. Connect remote or local ground |
| 14 | RSo | Output of Remote sense amp |
| 11 | PS | Phase setting pin. Connect resistor AGnd to set Master/Slave as well as number of devices in parallel to determine relative phasing |
| 24 | Fault# | Share fault information with other paralleled devices. Active low |
| 20 | Ishare | Current share pin |
| 1-4, 51, 52 | PVin | Input supply for the power MOSFETs |

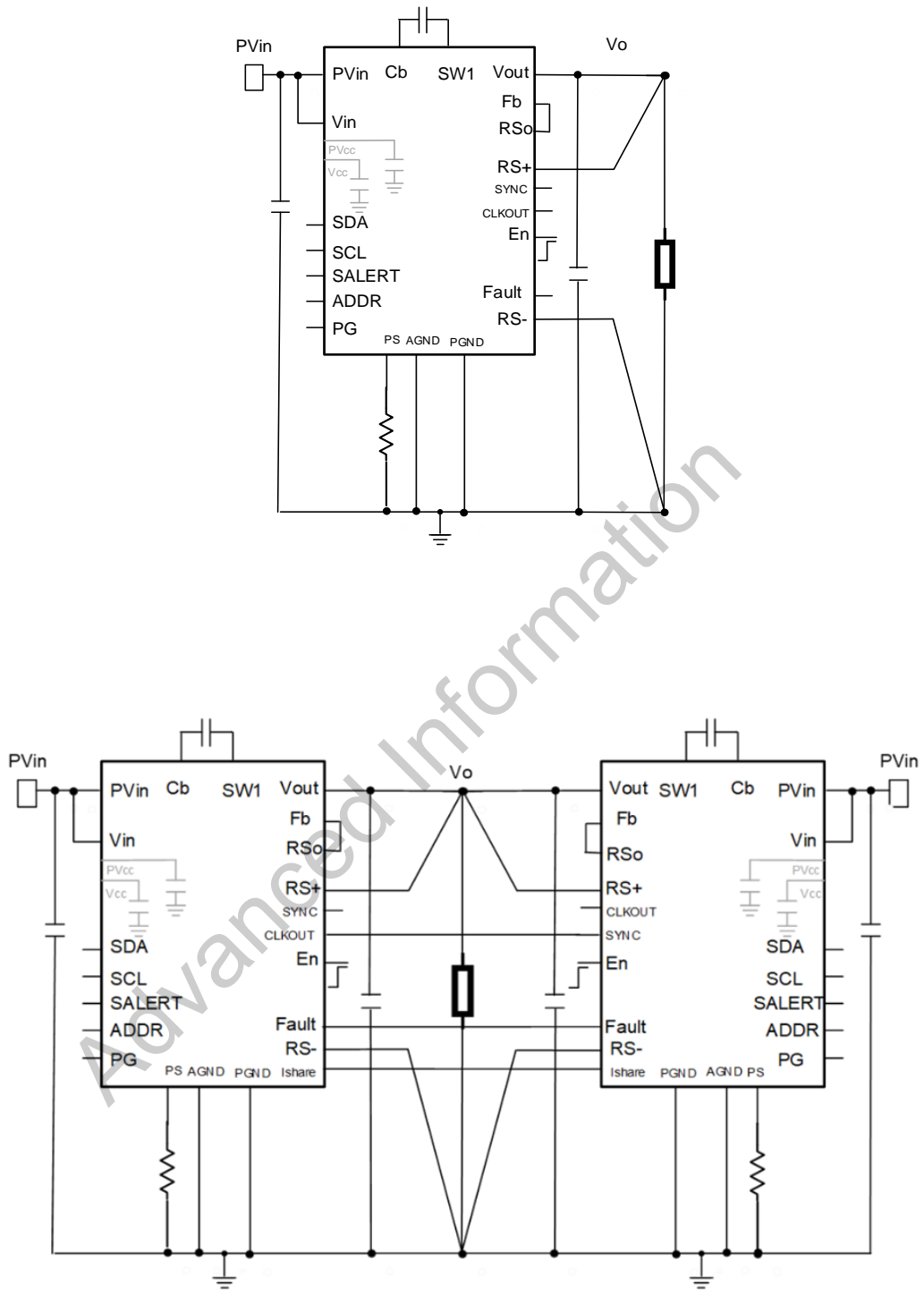# Block diagram
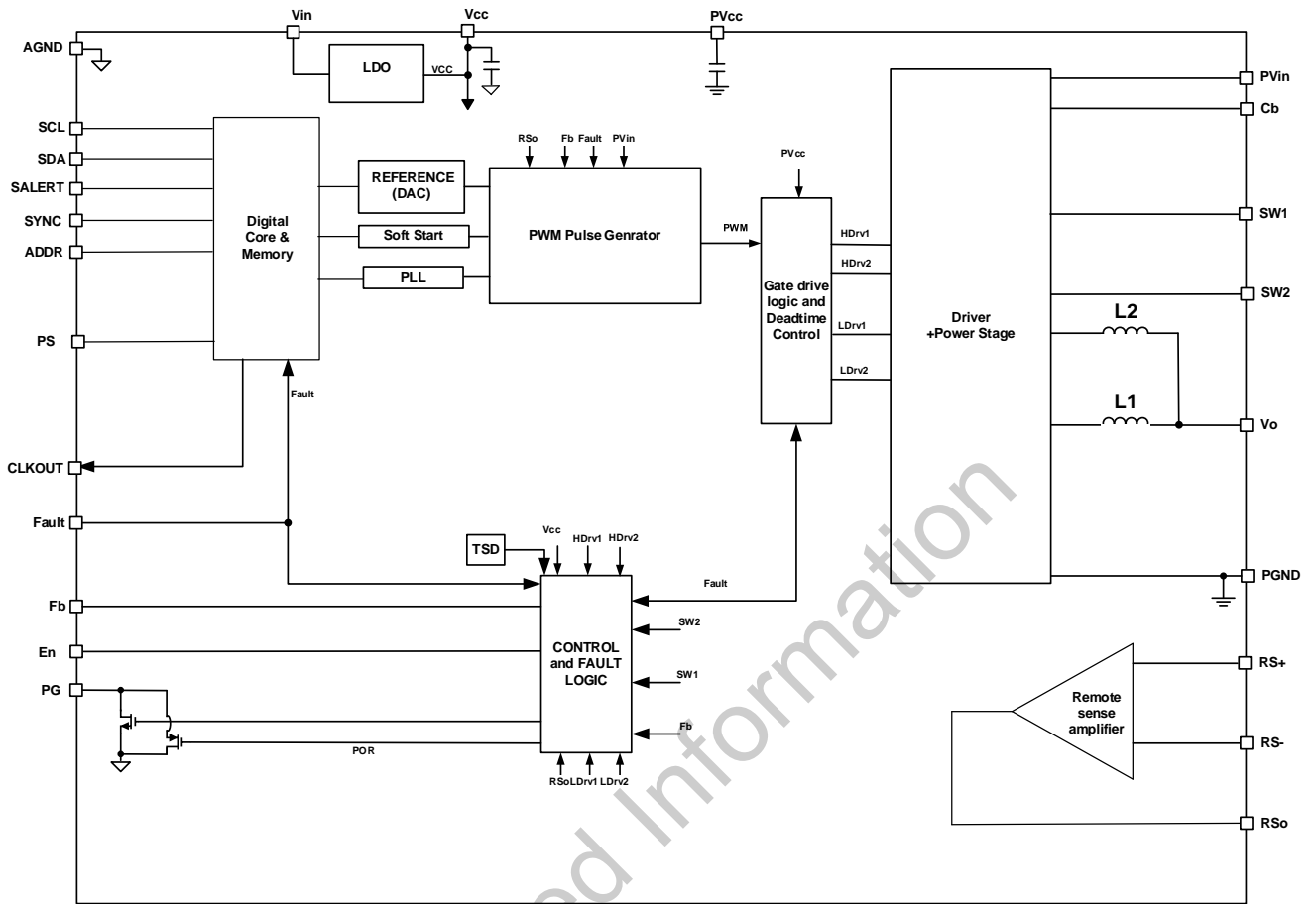


*Figure 3   FS1525 µPOL™*

*Figure 4    Applications circuits for single-phase and two-phase configuration*

# Absolute maximum ratings

**Warning:** Stresses beyond those shown may cause permanent damage to the FS1525.

**Note:** Functional operation of the FS1525 is not implied under these or any other conditions beyond those stated in the FS1525 specification.

| Reference | Range |
|---|---|
| PV$_{IN}$, V$_{IN}$, En to PGnd (Note 2), CB to SW1 | -0.3V to 18V |
| V$_{CC}$ to PGnd (Note 1) | -0.3V to 6V |
| SW1, SW2 | -0.3V to 15V |
| Fb and other I/Os to AGnd (Note1) | -0.3V to V$_{CC}$ |
| PG to AGnd (Note 1) | -0.3V to V$_{CC}$ |
| PGnd to AGnd | -0.3V to +0.3V |
| ESD Classification (HBM JESD22-A114) | 2kV |
| Moisture Sensitivity Level | MSL 3 (per JEDEC J-STD-020D) |

| Thermal Information | Range |
|---|---|
| Junction-to-Ambient Thermal Resistance Θ$_{JA}$ | 10.5°C/W |
| Junction to PCB Thermal Resistance Θ$_{J-PCB}$ | 1.4°C/W |
| Storage Temperature Range | -55°C to 150°C |
| Junction Temperature Range | -40°C to 150°C |

**Note:** Θ$_{JA}$ : FS1525 evaluation board and JEDEC specifications JESD 51-2A
Θ$_{J-c\ (bottom)}$ : JEDEC specification JESD 51-8

# Order information

## Package details

The FS1525 uses a µPOL™ 6.9mm x 7.6mm package delivered in tape-and-reel format, with 1250 devices on a reel.

## Standard part number

| | Part numbers |
|---|---|
| V<sub>OUT</sub> | 1250 devices on a reel |
| 0.60 | FS1525-0600-AL |

# Recommended operating conditions

| Definition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Voltage Range with External $V_{CC}$ (Note 3, Note 5) | $PV_{IN}$ | $6*V_{OUT}$ | 16 | |
| Input Voltage Range with Internal LDO (Note 4, Note 5) | $PV_{IN}$, $V_{IN}$ | $6*V_{OUT}$ | 16 | V |
| Supply Voltage Range (Note 2) | $V_{CC}$ | 4.5 | 5.5 | |
| Output Voltage Range | $V_{OUT}$ | 0.6 | 1.8 | |
| Continuous Output Current Range | $I_O$ | 0 | 25 | A |
| Operating Junction Temperature | $T_J$ | -40 | 125 | °C |

# Electrical characteristics

| ELECTRICAL CHARACTERISTICS | | | | | | |
|---|---|---|---|---|---|---|
| Unless otherwise stated, these specifications apply over: $6*V_{OUT} < PV_{IN} < 16V$, $4.5V < V_{IN} < 16V$, $0°C < T < 125°C$ | | | | | | |
| Typical values are specified at $T_A = 25°C$ | | | | | | |
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| **Supply Current** | | | | | | |
| $V_{IN}$ Supply Current (Standby) | $I_{IN (STANDBY)}$ | Enable low | | TBS | | |
| $V_{IN}$ Supply Current (Static) | $I_{IN (STATIC)}$ | No switching, En = 2V | | TBS | | mA |
| $V_{IN}$ Supply Current (Dynamic) | $I_{IN (DYN)}$ | En high, $V_{IN}$ = 12V, $F_{SW}$ =625kHz | | TBS | | |
| **Soft-Start** | | | | | | |
| Soft-Start time | $SS_{RATE}$ | Default (Note 7), $V_{OUT}$ = 0.6V, $T_{ON\_RISE}$=2ms | | 0.25 | | V/ms |
| **Output Voltage** | | | | | | |
| Output Voltage Range | $V_{OUT}$ (default) | | | 0.6 | | V |
| | range | | 0.6 | | 1.8 | V |
| | Resolution | | | 5 | | mV |
| Accuracy | | $T_J$ = 25°C, $V_{OUT}$ = 0.6V | | ±0.5 | | % |
| | | $0°C < T_J < 85°C$ (Note 6) | -1 | | +1 | |
| **On-Time Timer Control** | | | | | | |
| On Time | $T_{ON}$ | $V_{IN}$ = 12V, $V_{OUT}$ = 0.6V, $F_{SW}$ = 625kHz | | TBS | | |
| Minimum On-Time | $T_{ON(MIN)}$ | (Note 7) | | 50 | | ns |
| Minimum Off-Time | $T_{OFF(MIN)}$ | $T_J$=25°C, $F_{SW}$= 625kHz, $PV_{IN}$=2V | | 1200 | 1300 | |
| **Internal Low Drop-Out (LDO) Regulator** | | | | | | |
| LDO Regulator Output Voltage | $V_{CC}$ | $5.5V < V_{IN}$ = 16V, 0 – TBSmA | 4.9 | 5.2 | 5.4 | V |
| | | $4.5V ≤ V_{IN} < 5.5V$, 0 – TBSmA | 4.4 | | | |
| Line Regulation | $V_{LN}$ | $5.5V < V_{IN}$ = 16V, 0 – TBS mA | | | 30 | mV |
| Load Regulation | $V_{LD}$ | 0 – TBSmA | | | 100 | |
| Short Circuit Current | $I_{SHORT}$ | (Note 7) | | TBS | | mA |

**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, these specifications apply over: $6*V_{OUT} < PV_{IN} < 16V$, $4.5V < V_{IN} < 16V$, $0°C < T < 125°C$

Typical values are specified at $T_A = 25°C$

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Thermal Shut-Down** | | | | | | |
| Thermal Shut-Down | Default | | | 145 | | °C |
| Hysteresis | | | | 25 | | |
| **Under-Voltage Lock-Out** | | | | | | |
| $V_{CC}$ Start Threshold | $V_{CC}$_UVLO(START) | $V_{CC}$ Rising Trip Level | 4.0 | 4.2 | 4.4 | V |
| $V_{CC}$ Stop Threshold | $V_{CC}$_UVLO(STOP) | $V_{CC}$ Falling Trip Level | 3.6 | 3.8 | 4.1 | |
| Enable Threshold | En(HIGH) | Ramping Up | 1.14 | 1.20 | 1.36 | |
| | En(LOW) | Ramping Down | 0.90 | 1.00 | 1.06 | |
| Input Impedance | $R_{EN}$ | | 500 | 1000 | 1500 | kΩ |
| **Current Limit** | | | | | | |
| Current Limit Threshold | $I_{OC}$ (default) | $T_J$ = 25°C | | 32 | | A |
| | $I_{OC}$ (range) | | 15 | | 32 | |
| Hiccup Blanking Time | $T_{BLK(HICCUP)}$ | | | 20 | | ms |
| **Over-Voltage Protection** | | | | | | |
| Output Over-Voltage Protection Threshold | $V_{OVP}$ (default) | OVP Detect (Note 7) | 115 | 120 | 125 | Fb% |
| | $V_{OVP}$ (range) | | 105 | | 120 | |
| | $V_{OVP}$ (resolution) | | | 5 | | |
| Output Over-voltage Protection Delay | $T_{OVPDEL}$ | | | 5 | | µs |
| **Remote Sense Differential Amplifier** | | | | | | |
| Differential Gain | $A_{diff}$ | | | 1 | | V/V |
| Input Offset Voltage | $V_{os}$ | Rso=0.6V, No Load | | 0 | | mV |
| Output Source Current | $I_{src}$ | RS+ = TBS V, RS- = 0V, Rso = TBS V | | 4.3 | | mA |
| Output Sink Current | $I_{snk}$ | RS+ = 0V, RS- = 0.6V, Rso = 0.6V | | 0.53 | | mA |
| **Power Good (PG)** | | | | | | |
| Power Good Upper Threshold | $V_{PG(UPPER)}$ (default) | $V_{OUT}$ Rising | | 85 | | Fb% |
| Power Good Hysteresis | $V_{PG(LOWER)}$ | $V_{OUT}$ Falling | | 5 | | |
| Power Good Sink Current | $I_{PG}$ | PG = 0.6V, En = 2V | 2.5 | 5 | | mA |
| Power Good Voltage Low | $V_{PG(LOW)}$ | $V_{IN}$ = $V_{CC}$ = 0V, $R_{PUL-UP}$ = 50kΩ @ 3.3V | | 0.3 | 0.5 | V |
| **Telemetry** | | | | | | |
| Input voltage reporting accuracy | $PV_{IN}$_report_pc | $PV_{IN}$=12V, $T_J$ = 25°C | -0.8 | | 0.8 | % |
| | | 5V<$PV_{IN}$<16V, -40°C < $T_J$ <125°C | TBS | | TBS | mV |
| Output voltage reporting accuracy | $V_{OUT}$_report_pc | $V_{OUT}$ = $V_{FB}$ =0.6V, $T_J$ = 25°C | -2.5 | | 2.5 | % |
| | | 0.6< $V_{FB}$ <1.8, -40°C < $T_J$ <125°C | TBS | | TBS | mV |
| Output current reporting accuracy | Iout_report_pc | | TBS | | TBS | A |
| Temperature reporting accuracy | T_report_acc | -40°C < $T_J$ <125°C (Note 7) | -10 | | 10 | °C |

**ELECTRICAL CHARACTERISTICS**

**Unless otherwise stated, these specifications apply over: 6\*V$_{OUT}$ < PV$_{IN}$ = V$_{IN}$ < 16V, 0°C < T < 125°C**

**Typical values are specified at T$_A$ = 25°C**

| Parameter<br><br>I²C parameters | Symbol | Conditions<br><br>(Note 7 for all parameters) | Fast-mode | | Fast-mode Plus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| I²C bus voltage | V$_{BUS}$ | | 1.8 | 5.5 | 1.8 | 5.5 | V |
| LOW-level input voltage | V$_{IL}$ | | −0.5 | 0.3V$_{BUS}$ | −0.5 | 0.3V$_{BUS}$ | |
| HIGH-level input voltage | V$_{IH}$ | | 0.7V$_{BUS}$ | | 0.7V$_{BUS}$ | | |
| Hysteresis | V$_{HYS}$ | | 0.05V$_{BUS}$ | | 0.05V$_{BUS}$ | | |
| LOW-level output voltage 1 | V$_{OL1}$ | (open-drain or open-collector) at 3mA sink current; V$_{DD}$ > 2 V, | 0 | 0.4 | 0 | 0.4 | |
| LOW-level output voltage 2 | V$_{OL2}$ | (open-drain or open-collector) at 2mA sink current; V$_{DD}$ ≤ 2 V, | 0 | 0.2V$_{BUS}$ | 0 | 0.2V$_{BUS}$ | |
| LOW-level output current | I$_{OL}$ | V$_{OL}$ = 0.4 V, | 3 | - | 3 | - | mA |
| | | V$_{OL}$ = 0.6 V | 6 | - | 6 | - | |
| Output fall time | T$_{OF}$ | From V$_{IHmin}$ to V$_{ILmax}$ | 20 × (V$_{BUS}$/5.5 V) | 250 | 20 × (V$_{BUS}$/5.5 V) | 125 | ns |
| Pulse width of spikes that must be suppressed by the input filter | T$_{SP}$ | | 0 | 50 | 0 | 50 | ns |
| Input current each I/O pin | I$_I$ | | −10 | 10 | −10 | 10 | μA |
| Capacitance for each I/O pin | C$_I$ | | - | 10 | - | 10 | pF |
| SCL clock frequency | F$_{SCL}$ | | 0 | 400 | 0 | 1000 | kHz |
| Hold time (repeated) START condition | T$_{HD;STA}$ | After this time, the first clock pulse is generated | 0.6 | - | 0.26 | - | μs |
| LOW period of the SCL clock | T$_{LOW}$ | | 1.3 | - | 0.5 | - | |
| HIGH period of the SCL clock | T$_{HIGH}$ | | 0.6 | - | 0.26 | - | |
| Set-up time for a repeated START condition | T$_{SU;STA}$ | | 0.6 | - | 0.26 | - | |
| Data hold time | T$_{HD;DAT}$ | I²C-bus devices | 0 | - | 0 | - | |
| Data set-up time | T$_{SU;DAT}$ | | 100 | - | 50 | - | ns |
| Rise time of SDA and SCL signals | T$_R$ | | 20 | 300 | - | 120 | |
| Fall time of SDA and SCL signals | T$_F$ | | 20 × (V$_{DD}$/5.5 V) | 300 | 20 × (V$_{DD}$/5.5 V) | 120 | |
| Set-up time for STOP condition | T$_{SU;STO}$ | | 0.6 | - | 0.26 | - | μs |
| Bus free time between a STOP and START condition | T$_{BUF}$ | | 1.3 | - | 0.5 | - | |
| Capacitive load for each bus line | C$_B$ | | - | 400 | - | 550 | pF |
| Data valid time | T$_{VD;DAT}$ | | - | 0.9 | - | 0.45 | μs |
| Data valid acknowledge time | T$_{VD;ACK}$ | | - | 0.9 | - | 0.45 | |

**ELECTRICAL CHARACTERISTICS**

**Unless otherwise stated, these specifications apply over: 6\*V$_{OUT}$ < PV$_{IN}$ = V$_{IN}$ < 16V, 0°C < T < 125°C**
**Typical values are specified at T$_A$ = 25°C**

| Parameter | Symbol | Conditions | Fast-mode | | Fast-mode Plus | | Unit |
|---|---|---|---|---|---|---|---|
| I²C parameters | | (Note 7 for all parameters) | Min | Max | Min | Max | |
| Noise margin at the LOW level | V$_{NL}$ | For each connected device, including hysteresis | 0.1V$_{DD}$ | - | 0.1V$_{DD}$ | - | V |
| Noise margin at the HIGH level | V$_{NH}$ | | 0.2V$_{DD}$ | - | 0.2V$_{DD}$ | - | |
| SDA timeout | T$_{TO}$ | | 200 | | 200 | | µs |

For supported PMBus™ commands, see page 21.

**Notes**

1   PGnd pin and AGnd pin are connected together
2   Must not exceed 6V
3   V$_{IN}$ is connected to V$_{CC}$ to bypass the internal Low Drop-Out (LDO) regulator
4   V$_{IN}$ is connected to PV$_{IN}$ (for single-rail applications with PV$_{IN}$=V$_{IN}$=4.5V-5.5V)
5   Maximum switch node voltage should not exceed 15V
6   Cold temperature performance guaranteed by correlation using statistical quality control but not tested in production
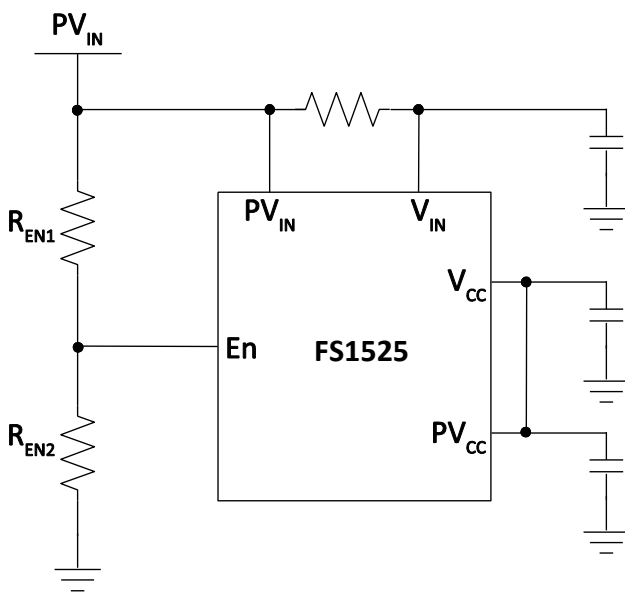7   Guaranteed by design but not tested in production

*Figure 5 Single supply configuration: internal LDO regulator, adjustable PV$_{IN}$_UVLO*
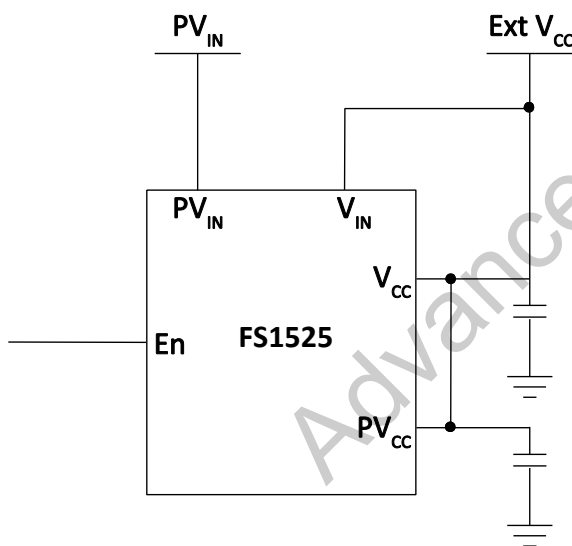


*Figure 6 Using an external bias voltage*

## I²C base address and offsets

The FS1525 has user registers to set its I²C base address and PMBus™ base address. The default I²C base address is 0x10, and the default PMBus™ base address is 0x70. An offset of 0–15 is then defined by connecting the ADDR pin to the AGnd pin, either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I²C address to set the address at which the I²C master device will communicate with the FS1525. The same offset is added to the base PMBus™ address to determine the PMBus™ address at which PMBus™ communication will be established.

To select offsets of 0–15, connect the pins as follows:

- **0** – 0Ω (short ADDR to AGnd)
- **+1** – 1.13kΩ
- **+2** – 1.87kΩ
- **+3** – 2.61kΩ
- **+4** – 3.4kΩ
- **+5** – 4.12kΩ
- **+6** – 4.87kΩ
- **+7** – 5.62kΩ
- **+8** – 6.34kΩ
- **+9** – 7.15kΩ
- **+10** – 7.87kΩ
- **+11** – 8.66kΩ
- **+12** – 9.31kΩ
- **+13** – 10.2kΩ
- **+14** – 11kΩ
- **+15** – 12.1kΩ

**Note:** Do not use the 7-bit address 0x0C; this corresponds to the Alert Response Address in the SMBus™ protocol.

## Soft-start and target output voltage

The FS1525 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When $V_{CC}$ exceeds its start threshold ($V_{CC}$\_ULVO$_{(START)}$), the FS1525 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete, the internal soft start begins to ramp towards the set reference voltage at a rate determined by the TON_RISE registers (corresponding to the TON_RISE command), provided these conditions are met:

a) A valid enable signal is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage $PV_{IN}$, and $PV_{IN}$ UVLO threshold corresponding to the VIN_ON registers).

b) The flying capacitor Cb has been charged to $PV_{IN}/2$ by the internal pre-charge circuit. This is necessary to ensure that when the device starts to switch, it does so with balanced $PV_{IN}/2$ voltages across all FETs.

During initial start-up, the FS1525 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Minimum values for on-time, off-time on page 16). On-time is increased until $V_{OUT}$ reaches the target value defined by the VOUT_COMMAND registers. For proper start-up operation of the FS1525, fitting a 100Ω resistor in parallel with the output capacitors ($C_{OUT}$) is not mandatory, but recommended.
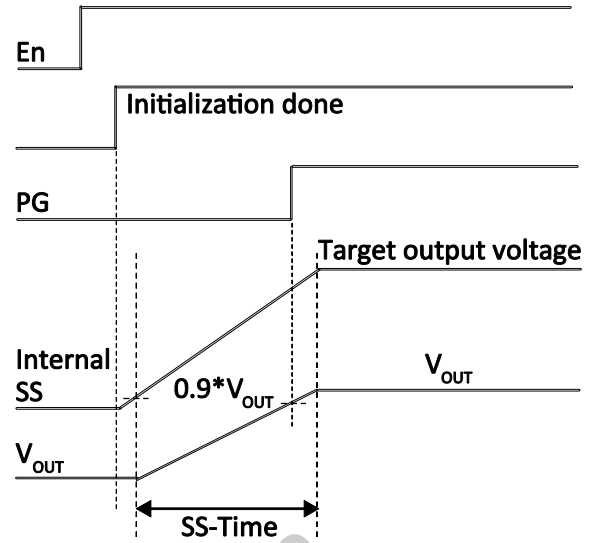


*Figure 7  Theoretical operational waveforms during soft-start*

Over-current protection (OCP) and over-voltage protection (OVP) are enabled during soft-start to protect the FS1525 from short circuits and excess voltages respectively.

A resistor divider may be used with a standard FS1525-0600 device to set the desired output voltage (Figure 8). This gives system designers the flexibility to design all the power rails in the system across the entire output voltage range (0.6–1.8V) using a single part.
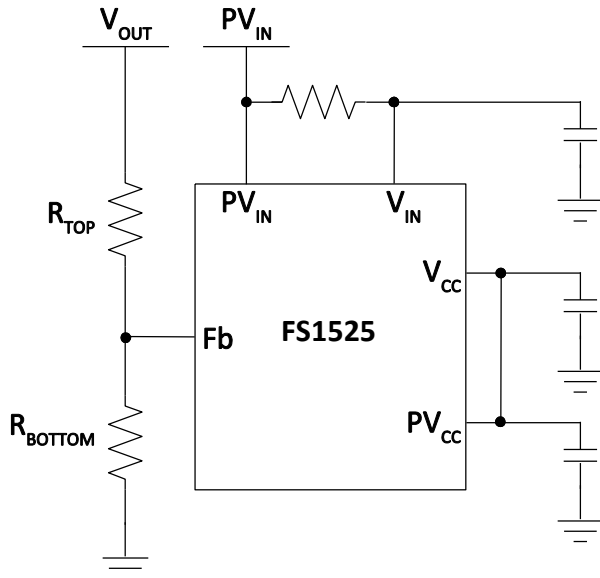


*Figure 8 Setting the output voltage with an external resistor divider*

The following equation may be used to set the output voltage:

$$V_{out} = V_{FB}\left(1 + \frac{R_{top} + \frac{R_{top}R_{bottom}}{41.3}}{R_{bottom}}\right)$$

Where $R_{top}$ and $R_{bottom}$ are in kΩ.

$R_{top}$ is recommended to be 1 kΩ and a feedforward capacitance of 1nF is recommended in parallel with it.

Instead of an external resistor divider, the output voltage can be set using I²C/PMBus™ commands (see page 21) or the corresponding user registers. FS1525 supports this command with a resolution of 1/1024V. Alternatively the initial output voltage

may be set using the PS resistor to select from a pre-programmed setting in one of eight user register pairs (see PS section).

## Shut-down mechanisms

The FS1525 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*
  A valid hard-disable is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PV$_{IN}$, and PV$_{IN}$ UVLO threshold corresponding to the VIN_ON registers). Both drivers switch off and soft-start is pulled down instantaneously.

- *Soft-Stop or controlled ramp down*
  A valid soft-off request is recognized (as defined by the Enable pin, Operation register and ON_OFF_CONFIG register). Then, following a delay corresponding to the TOFF_DELAY registers, the SS signal falls to 0 in a time defined by the TOFF_FALL registers; the drivers are disabled only when it reaches 0. The output voltage follows the SS signal down to 0.

By default, the device is configured for hard shut-down. Shut-down with PV$_{IN}$ is always a hard shut-down.

## Phase setting pin (PS)

The PS pin on the FS1525 is a multi-function pin.

a) In applications that require operating multiple FS1525 devices in parallel, the phase between adjacent modules (and hence the number of devices) may be selected by using the appropriate resistor from PS to AGnd. In these applications, this pin can also be used to assign "master" status to one of the parallel modules

b) Certain settings of the PS resistor, indicated in the table below, can be used to set the desired switching frequency of operation. It is

recommended that the switching frequency be set dependent on the output voltage such that

$$750\, kHz \times V_{OUT} \le F_{sw} \le 1 MHz \times V_{OUT}$$

c) Certain settings of the PS resistor, indicated in the table below can be used to set the initial output voltage at startup. Any subsequent PMBus commands that set the output voltage will then override this.

| R_PS (kΩ) | Master/ Slave | Phase (⁰) | Initial Vout (V) | Fsw (MHz) |
|---|---|---|---|---|
| 0 | Master | 0 | 0.6 | Fsw table |
| 1.13 | Slave | 180 | 0.6 | Sync to master |
| 1.87 | Slave | 120 | 0.6 | Sync to master |
| 2.61 | Slave | 90 | 0.6 | Sync to master |
| 3.4 | Slave | 72 | 0.6 | Sync to master |
| 4.12 | Slave | 60 | 0.6 | Sync to master |
| 4.87 | Slave | 51.4 | 0.6 | Sync to master |
| 5.62 | Slave | 45 | 0.6 | Sync to master |
| 6.34 | Master | 0 | 0.6 | 1.5 |
| 7.15 | Master | 0 | 1.2 | 1.25 |
| 7.87 | Master | 0 | 0.6 | 1.04 |
| 8.66 | Master | 0 | 0.6 | 0.892 |
| 9.31 | Master | 0 | 0.9 | 0.781 |
| 10.2 | Master | 0 | 0.85 | 0.694 |
| 11 | Master | 0 | 0.8 | 0.625 |
| 12.1 | Master | 0 | 0.7 | 0.568 |

| V_OUT range (V) | F_SW (MHz) |
|---|---|
| V_OUT < 0.85 | 0.625 |
| 0.85 < V_OUT < 1.1 | **0.781** |
| 1.1 < V_OUT < 2.1 | 1.25 |

## Minimum values for on-time, off-time and PV_IN

When input voltage is high relative to target output voltage, the Control MOSFETs are switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very small, the FS1525 operates with minimum on-time.

The maximum conversion ratio, on the other hand, is determined by two factors:

a) When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ($T_{OFF(MIN)}$). The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

b) To maintain balanced switching amplitudes in both phases (or to maintain the voltage on the Cb pin at 0.5*PV_IN), this topology requires there to be no overlap between the high sides of the two phases (unlike a conventional buck topology). This effectively imposes theoretical maximums of 50% on the duty cycle of each phase and 25% on the conversion ratio; in practice, allowing for circuit delays and dead-times, the conversion ratio must not exceed 16% at full load.

The maximum conversion ratio is affected by both system efficiency and load transient requirements. It is recommended that system designers validate the values in their own applications.

## Enable (En) pin

The Enable (En) pin has several functions:

- In the default setting of the ON_OFF_CONFIG command, it is used to switch the FS1525 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1525 being switched on unintentionally.

- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the $PV_{IN}$ voltage by a set of resistive dividers, $R_{EN1}$ and $R_{EN2}$ (Figure 5). Users can program the UVLO threshold voltage by selecting different ratios. A useful feature that stops the FS1525 regulating when $PV_{IN}$ is lower than the desired voltage, this may be used for finer control over the $PV_{IN}$ UVLO voltage levels than is provided by the VIN_ON/VIN_OFF commands.

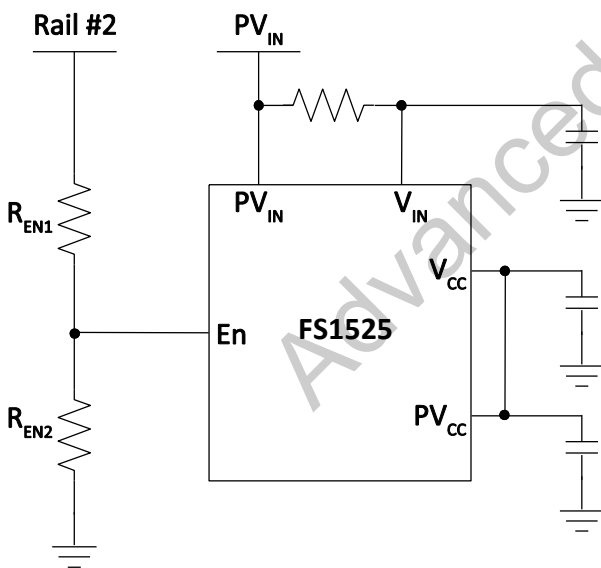- It can be used to monitor other rails for a specific power sequencing scheme (Figure 9).



*Figure 9   En pin used to monitor other rails for sequencing purposes*

## Over-current protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate over-current protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is defined by the IOUT_OC_FAULT_LIMIT command (or the corresponding user registers). The over-current limit may be programmed in 0.5A steps, up to a maximum of 37.5A.

The OCP threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1525 enters hiccup mode (Figure 10). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1525 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1525 remains in hiccup mode until the over-current fault is remedied. The FS1525 can be re-programmed to enter a latched shut-down mode on encountering an over-current fault.
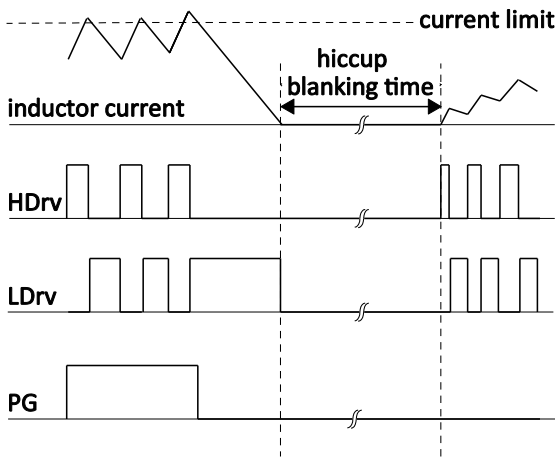
*Figure 10 Illustration of OCP in hiccup mode*

## Over-voltage protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the FB pin. When FB exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is defined by the VOUT_OV_FAULT_LIMIT command (or the corresponding user registers). This command allows the over-voltage level to be set relative to the output voltage, with a resolution of 1/1024 V. However, internally, these are rounded to one of four settings as shown in the table below.

| VOUT_OV_FAULT_LIMIT (% of VOUT_COMMAND) | Actual OVP Threshold (% of VOUT_COMMAND) |
|---|---|
| 100 < setting ≤ 105.4 | 105 |
| 105.4 < setting ≤ 110.1 | 110 |
| 110.1 < setting ≤ 114.8 | 115 |
| 114.8 < setting ≤ 100.1 | **120** |

The default setting is 120%. All the MOSFETs are switched off immediately and the PG pin is pulled low.

The MOSFETs remain latched off until reset by cycling either $V_{CC}$ or En. Figure 11 shows a timing diagram for over-voltage protection.
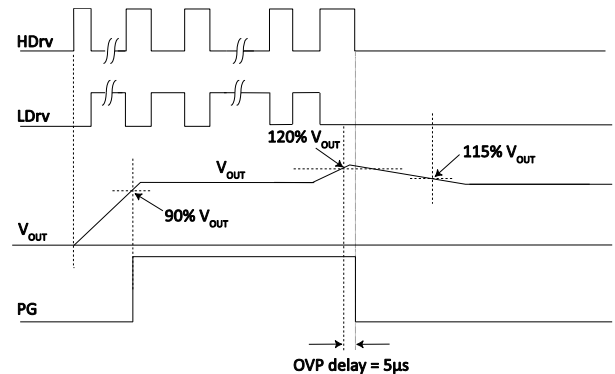


*Figure 11 Illustration of latched OVP*

The FS1525 provides output over-voltage and under-voltage warnings, as well as output under-voltage fault protection. These are set by three commands, respectively: VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT and VOUT_UV_FAULT_LIMIT (or the corresponding user registers). The mechanism for these thresholds is different from the over-voltage protection mechanism: the former rely on a digital comparison of the digitized and processed $V_{OUT}$ telemetry to the thresholds, whereas the latter relies on an all-analog signal path and an internal high-speed comparator.

## Over-temperature protection (OTP)

Temperature sensing is provided inside the FS1525. A programmable threshold set to a resolution of 1°C using the OT_FAULT_LIMIT command (or the corresponding user registers). When set lower than the fixed analog threshold (145°C), the programmable threshold determines the temperature at which the device trips, making a digital comparison of reported temperature (READ_TEMPERATURE) and OT_FAULT_LIMIT. When the reported temperature exceeds the programmable threshold, the device either continues power conversion (default) or goes into a latched shutdown, a behavior selected by reprogramming the OT_FAULT_RESPONSE PMBus command (or corresponding registers). Recovery requires either cycling Enable or the Operation command.

An over-temperature warning threshold may also be set using the OT_WARN_LIMIT command. It is typically set below the over-temperature fault threshold and may be used to provide an alarm through the PMBus™ SALERT# pin and the STATUS_TEMPERATURE register.

## Power Good (PG)

Power Good (PG) behavior is defined by the user register bits PGControl **and** by the POWER_GOOD_ON command. When the PGControl bit is set, the PMBus™ command may be used to set the upper power good threshold relative to the output voltage, with a resolution of 1/1024 V. However, internally, these are rounded to one of four settings as shown in the table below.

| POWER_GOOD_ON (% of VOUT_COMMAND) | Actual Power Good Threshold (% of VOUT_COMMAND) |
|---|---|
| 95.1 < threshold ≤ 85.1 | 80 |
| 79.6 < threshold ≤ 85.1 | 85 |

| POWER_GOOD_ON (% of VOUT_COMMAND) | Actual Power Good Threshold (% of VOUT_COMMAND) |
|---|---|
| 85.1 < threshold ≤ 89.8 | **90** |
| 89.81 < threshold ≤ 95.1 | 95 |

The default is 90%, so the PG signal will be asserted when the voltage at the Fb pin exceeds 90% of the VOUT_COMMAND setting (default 0.4V).

Hysteresis of 5% is applied to this, giving a lower threshold. When the voltage at the Fb pin drops below this lower threshold, the PG signal is pulled low.

### PGControl bit set to 1 (default)

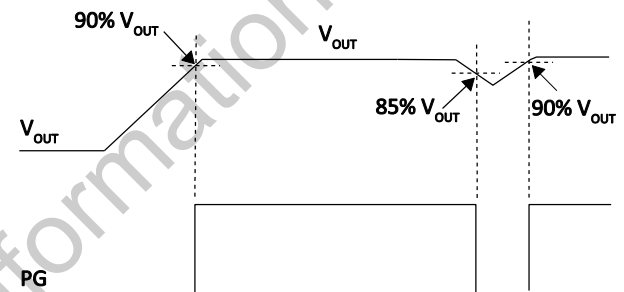Figure 12 shows PG behavior in this situation.



*Figure 12  PG signal when PGControl bit=1*

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- En and $V_{CC}$ are both above their thresholds
- No fault has occurred
  (including over-current, over-voltage and over-temperature)
- $V_{OUT}$ is within the target range
  (determined by continuously monitoring whether FB is above the PG threshold)

## PGControl bit set to 0

Figure 13 shows PG behavior in this situation.
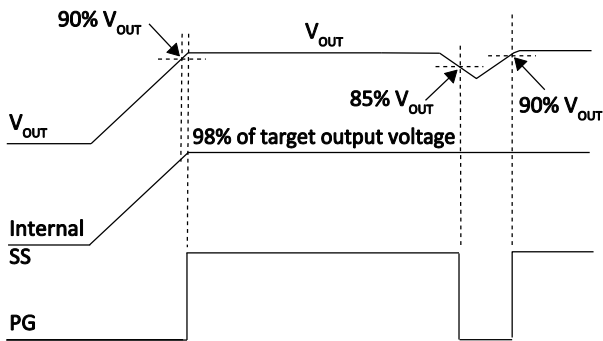


*Figure 13 PG signal when PGControl bit=0*

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after Fb is within 2% of target output voltage, not when Fb exceeds the upper PG threshold.

FS1525 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if $V_{CC}$ is low and the PG pin is pulled up to an external voltage not $V_{CC}$.

## Output Voltage Sensing (RS)

FS1525 offers a high performance true differential remote sensing to ensure output voltage accuracy by sensing cross the actual load to compensate any voltage drop due to high current. The remote sense amplifier has designed to have a fast slew rate with a source and sink current capability to respond to any transient event at the output. (More info will be added).

## Parallel Operation (RS)

FS1525 is capable of to operate in multi-module operation. In this mode all Modules are connected to the output voltage.

The Sync pin and Clkout pin take care of the synchronization among the Modules, and Ishare pin ensures the current sharing between the Modules. PS pin is used to set the number of modules and to allow interleaved operation with correct phase relationships between the parallel modules for optimum system level performance.

## Supported PMBus™ commands

| Code | Command | Code | Command |
|------|---------|------|---------|
| 01 | OPERATION | 55 | VIN_OV_FAULT_LIMIT |
| 02 | ON_OFF_CONFIG | 56 | VIN_OV_FAULT_RESPONSE |
| 03 | CLEAR_FAULTS | 58 | VIN_UV_WARN_LIMIT |
| 15 | STORE_USER_ALL | 5E | POWER_GOOD_ON |
| 16 | RESTORE_USER_ALL | 60 | TON_DELAY |
| 19 | CAPABILITY | 61 | TON_RISE |
| 1B | SMBALERT_MASK | 62 | TON_MAX_FAULT_LIMIT |
| 20 | VOUT_MODE | 63 | TON_MAX_FAULT_RESPONSE |
| 21 | VOUT_COMMAND | 64 | TOFF_DELAY |
| 24 | VOUT_MAX | 65 | TOFF_FALL |
| 25 | VOUT_MARGIN_HIGH | 78 | STATUS_BYTE |
| 26 | VOUT_MARGIN_LOW | 79 | STATUS_WORD |
| 27 | VOUT_TRANSITION_RATE | 7A | STATUS_VOUT |
| 29 | VOUT_SCALE_LOOP | 7B | STATUS_IOUT |
| 35 | VIN_ON | 7C | STATUS_INPUT |
| 36 | VIN_OFF | 7D | STATUS_TEMPERATURE |
| 39 | IOUT_CAL_OFFSET | 7E | STATUS_CML |
| 40 | VOUT_OV_FAULT_LIMIT | 88 | READ_VIN |
| 41 | VOUT_OV_FAULT_RESPONSE | 8B | READ_VOUT |
| 42 | VOUT_OV_WARN_LIMIT | 8C | **READ_IOUT** |
| 43 | VOUT_UV_WARN_LIMIT | 8D | READ_TEMPERATURE |
| 44 | VOUT_UV_FAULT_LIMIT | 98 | PMBUS_REVISION |
| 45 | VOUT_UV_FAULT_RESPONSE | 98 | PMBUS_REVISION |
| 46 | IOUT_OC_FAULT_LIMIT | 99 | MFR_ID |
| 47 | IOUT_OC_FAULT_RESPONSE | 9A | MFR_MODEL |
| 4A | IOUT_OC_WARN_LIMIT | 9B | MFR_REVISION |
| 4F | OT_FAULT_LIMIT | AD | IC_DEVICE_ID |
| 51 | OT_WARN_LIMIT | AE | IC_DEVICE_REV |

# Package description

The FS1525 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

As a result of these properties, the FS1525 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

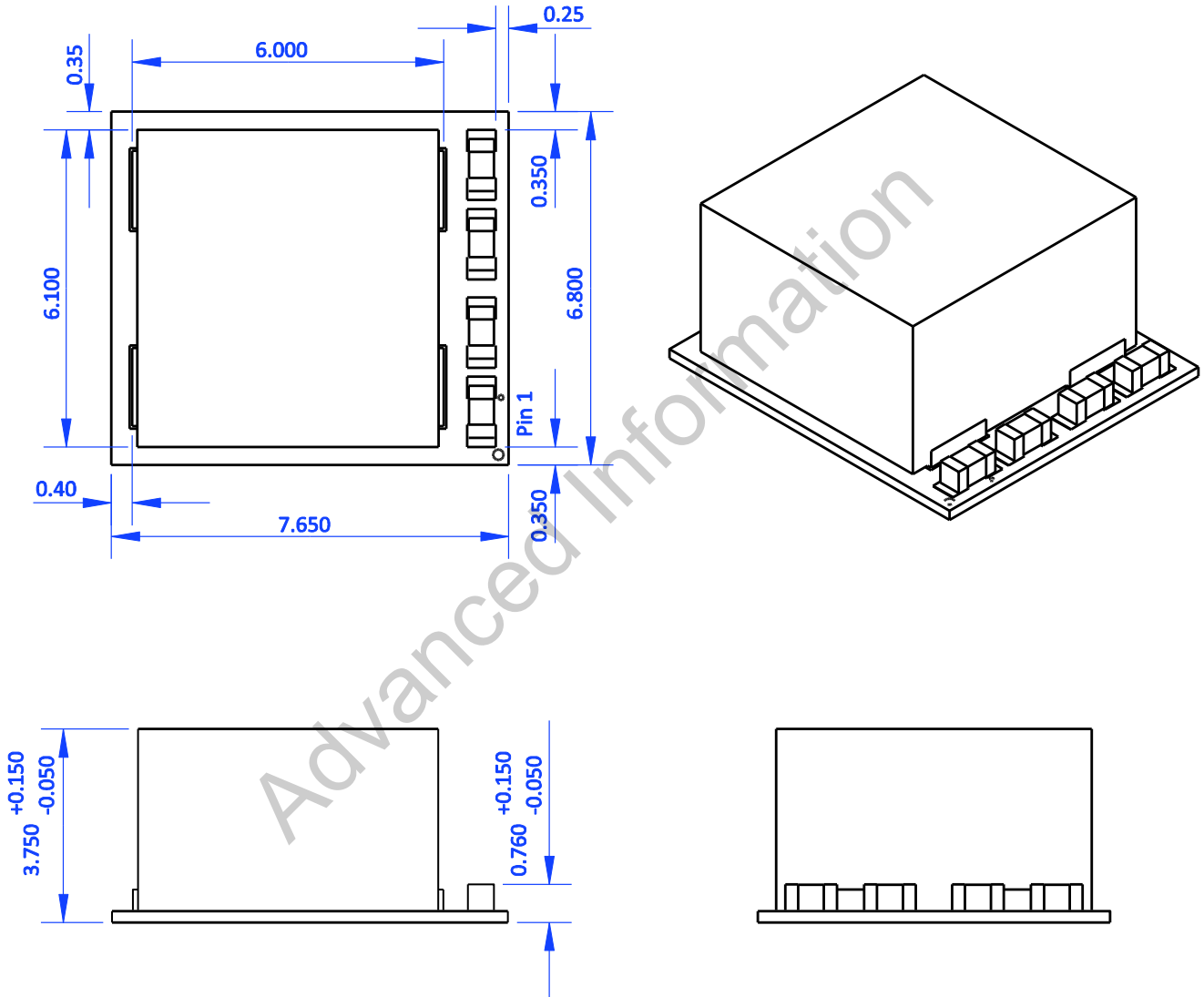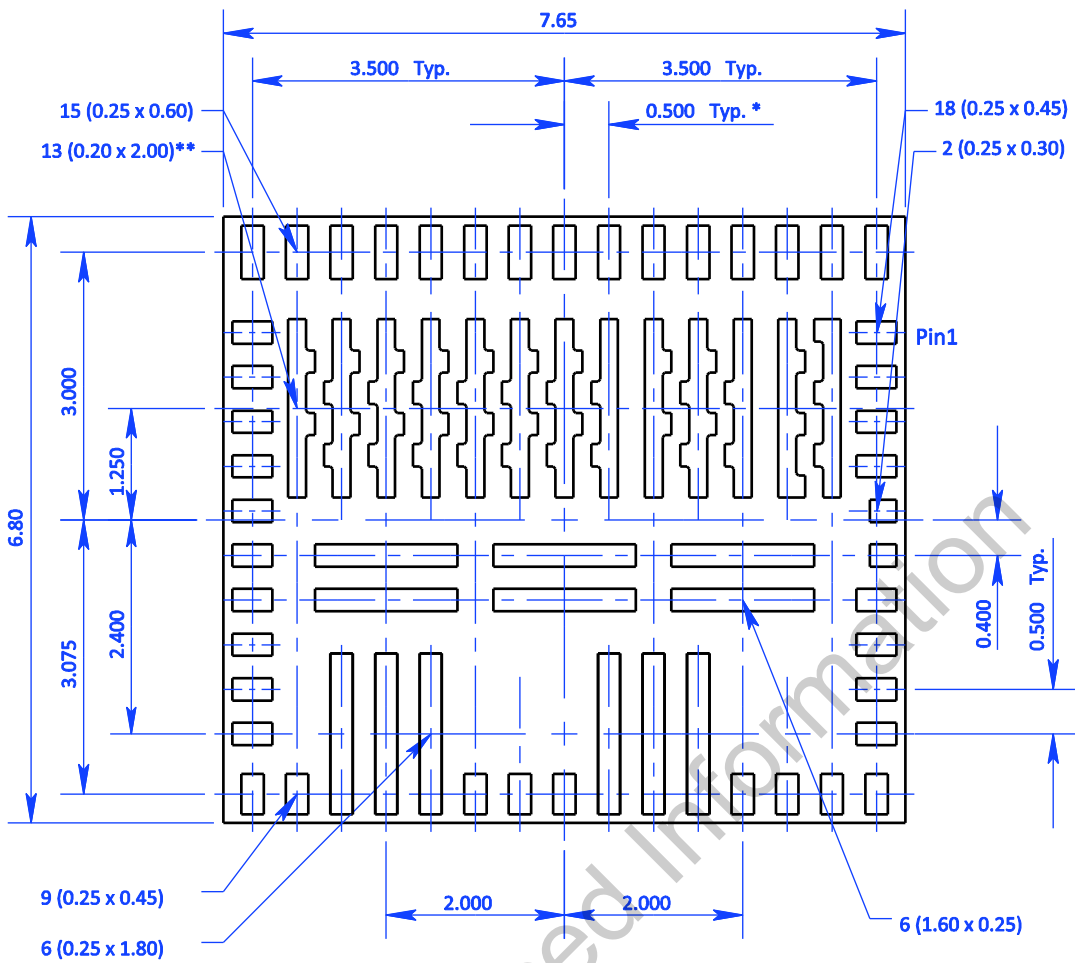**Note:** Refer to the Design Guidelines for more information about TDK's µPOL™ package series.
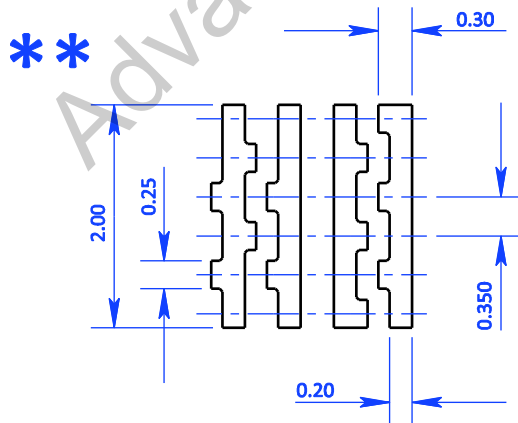


*Figure 14  Dimensioned drawings*

*Figure 15  Package footprint*

(to be supplied)

*Figure 16  Tape and reel pack*

# REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

## SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

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**REMINDER**

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The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety.

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This product is subject to a license from Power One, Inc. related to digital power technology patents owned by Power One, Inc. Power One, Inc. technology is protected by patents including:

AU 3287379M 3287437AA 3290643AA 3291357AA

CN 10371856C 10452610C 10458656C 10459360C 10465848C 1069332A 11124619A 11346682A 1685299A 1685459A 1685582A 1685583A 1698023A 1802619A

EP 1561156A1 1561268A2 1576710A1 1576711A1 1604254A4 1604264A4 1714369A2 1745536A4 1769382A4 1899789A2 1984801A2

US 20040246754 2004090219A1 2004093533A1 2004123164A1 2004123167A1 2004178780A1 2004179382A1 20050200344 20050223252 2005209373A1 20060061214 2006015619A1 20060174145 20070226526 20070234095 20070240000 20080052551 20080072080 20080186006 6741099 6788036 6936999 6949916 7000125 7049798 7069021 7080265 7249267 7266709 7315156 7372682 7373527 7394445 7456617 7459892 7493504 7526660

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