DESIGN GUIDELINES

Introduction

TDK's µPOL® range uses standardized packages to simplify application design. For each package series, this guideline provides recommendations on the design of the solder mask, copper pads and tracks, and solder stencil.

Packages are identified by area and footprint. So, for example, the P11F1 series is used for products with an area of approximately 11mm^2, with F1 identifying the first footprint in this series.

Each package is used by one or more products:

Package Code	Product Code
P11F1 series	FS1403; FS1404; FS1406; FS1603 Fs1604; FS1606; FS1703
P24F1 series	FS1412
P52F1 series	FS1525

All dimensions in this guideline are in mm.

P11F1 series

Package description

P11F1 series µPOL® products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 1), with the pads being higher than the surrounding substrate. The finish on the pads is ENIG (Electroless Nickel Immersion Gold), superseded by ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold) on later devices.

As a result of these properties, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Board layout

Note: Variations on the suggested PCB design may be applied, depending on application and capabilities.

Solder mask

Non-solder-mask-defined pads are recommended for this package.

In the design shown in Figure 2, the copper pads are 25µm larger on each side than the device footprint pads. The solder-mask openings are generally 75µm larger on each side than the copper pads; however, those marked with an 'A' are only 50µm larger.

Copper pads and tracks

PV_{IN} has been created as a single copper pad connected to all of the PV_{IN} device pads as shown in Figure 3. The main reason is to avoid using a combination of non-solder-mask-defined and solder-mask-defined pads, which can result in problems if positional tolerances are large.

For best results, the large PGnd and the adjacent large PV_{IN}* pad are connected through to the inner layers of the PCB using filled-via technology, µVia technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

* Effective thermal use of PV_{IN} requires the PV_{IN} pad to be connected to one or more of the inner layers.

Note: V_{SW} should be connected to an isolated pad on the PCB.

Solder stencil

The design shown in Figure 4 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

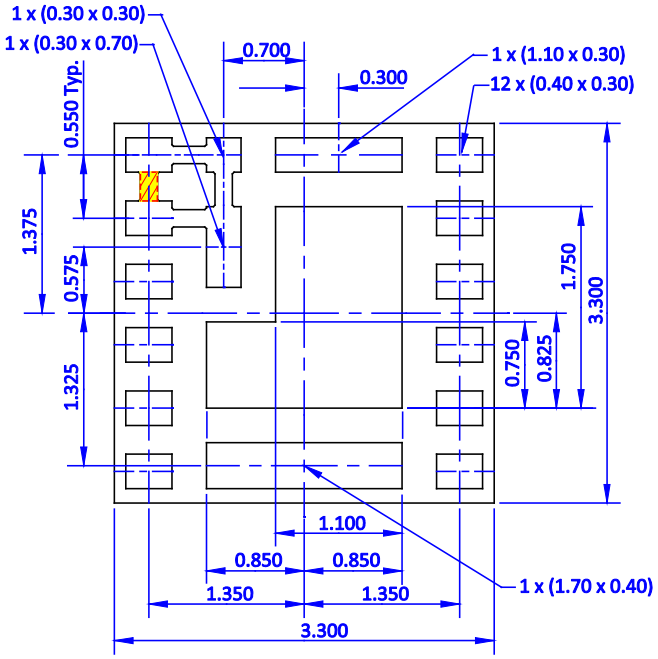
Flux residues

No-clean flux systems

The P11F1 series is compatible with all no-clean flux systems.

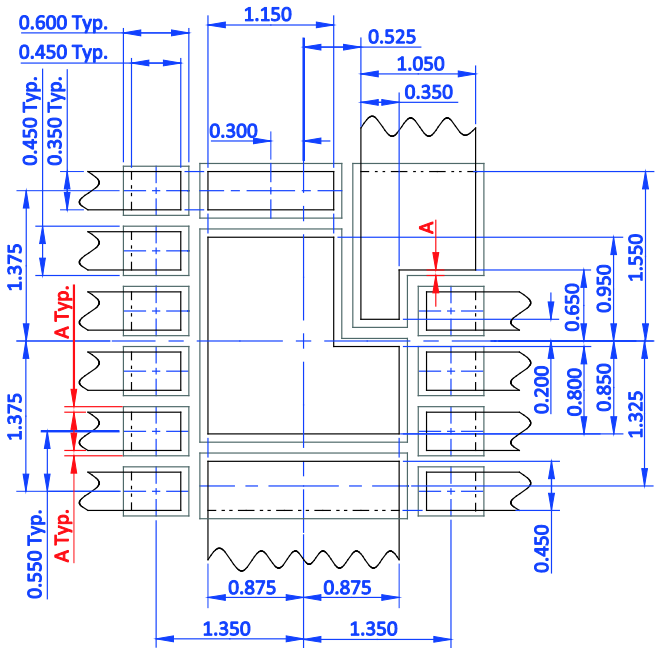
Cleanable flux systems

During some processes used to clean flux residues from PCBs, the outer coating of the inductor terminals on the P11F1 series has been observed to peel. Checking the compatibility of any such cleaning process before manufacturing starts is strongly advised.



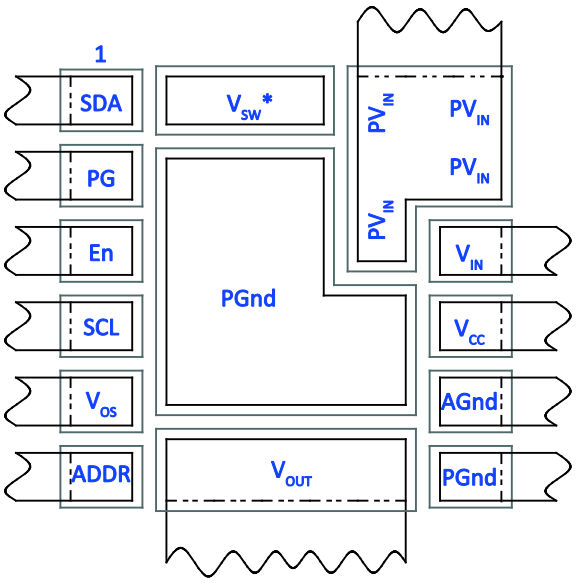
The highlighted bridge between pads is present on some devices and not on others. Originally designed to provide a more secure fixing, it has proved unnecessary.

Figure 1 Package footprint (bottom view)



Copper pads are 25µm larger on each side than device footprint pads. Solder-mask openings are 75µm larger on each side than copper pads (50µm where marked 'A').

Figure 2 PCB layout



* V_{SW} should be connected to an isolated pad on the PCB.

Figure 3 Copper pads and tracks

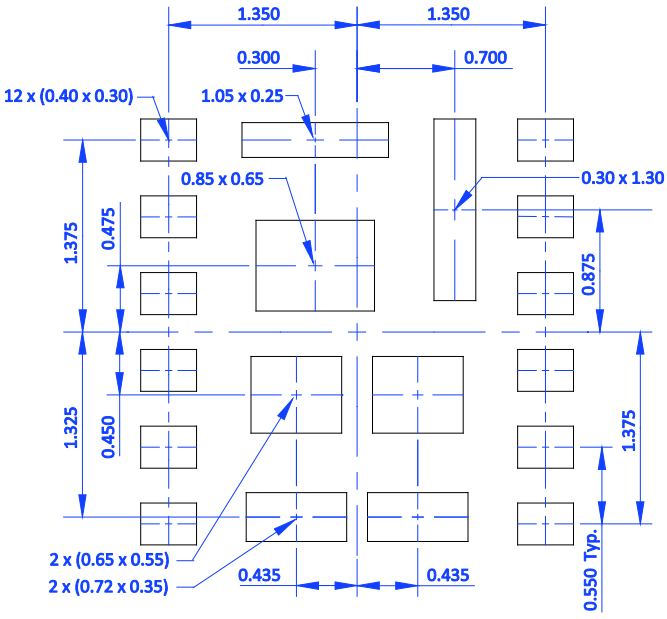


Figure 4 Solder stencil

Pick-and-place cycle

Center of mass

The pick point for the P11F1 series may be either the geometric center of the inductor or the center of mass of the package. Figure 5 and Figure 6 show the location of the center of mass.

Note: Position accurate to ±50µm.

Consistent results, without pick-and-place failures, have been achieved in assembly trials using the center of the inductor as the pick point and a round pick-up tool with an outside diameter of 2 mm. While the round pick-up tool used in the trials was adequate, a rectangular pick-up tool would be ideal for the package geometry.

Self-alignment

In the assembly trials, devices were deliberately misplaced on the X-Y axis and rotated. Even when misplaced by 200µm and rotated by up to 5°, the devices demonstrated excellent self-alignment properties.

Side 1 placement

If required, the P11F1 series can be placed on the first side of the PCB. In the assembly trials, no movement of the package, or of the passive components within it, was detected between the first and second reflow processes. Devices remained in place during the second reflow process without any adhesive. The surface tension of the molten solder is sufficient to hold in place the very low mass of the package (49 mg ± 5%).

Note: The trials also included tests with adhesive (information is available on request).

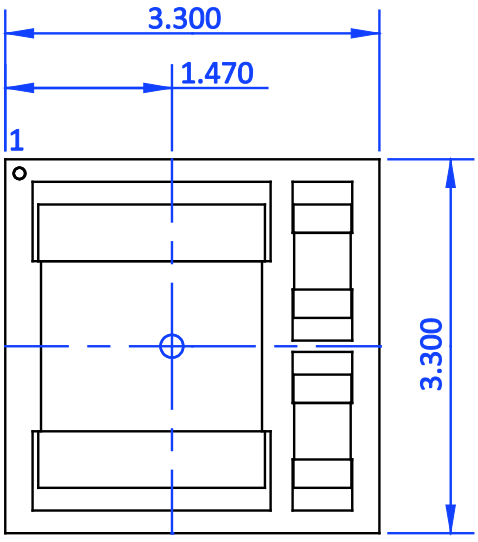


Figure 5 Center of mass (top view)

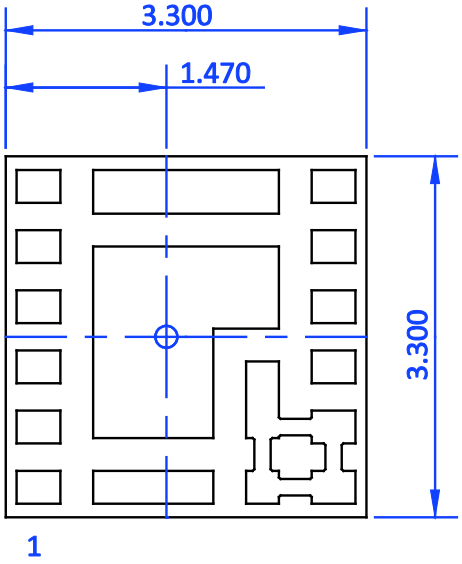


Figure 6 Center of mass (bottom view)

P24F1 series

Package description

P24F1 series µPOL® products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 7), with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

As a result of these properties, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Board layout

Solder mask

Non-solder-mask-defined pads are recommended for this package.

Copper pads and tracks

The copper layer of the board has been biased by 25µm on each side. The copper area should ideally be the same size or just little larger than the device footprint on the top surface. The solder mask should not extend onto the copper surface under the device footprint.

For best results, the large PGnd and the adjacent large PV_{IN}* pad are connected through to the inner layers of the PCB using filled-via technology, µVia technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

* Effective thermal use of PV_{IN} requires the PV_{IN} pad to be connected to one or more of the inner layers.

Note: CB is usually connected to an isolated pad on the PCB. However, if extra capacitance is required, this connection may be extended and extra capacitors connected between CB and V_{SW1}.

The smaller PV_{IN} pad is not electrically connected to the device internally.

Solder stencil

The design shown in Figure 10 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

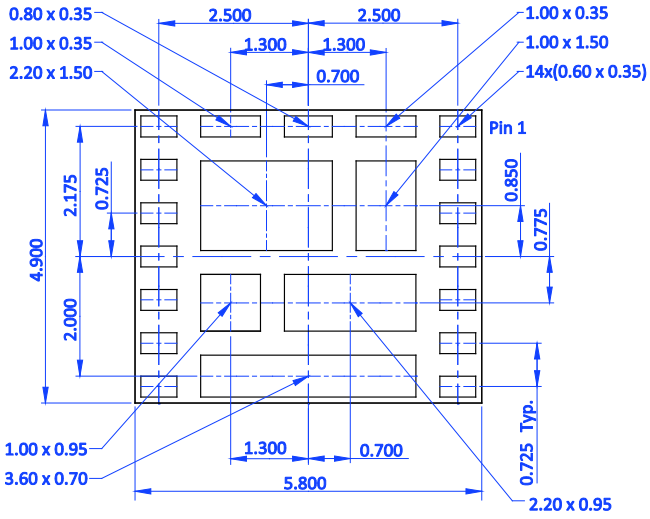


Figure 7 Package footprint (bottom view)

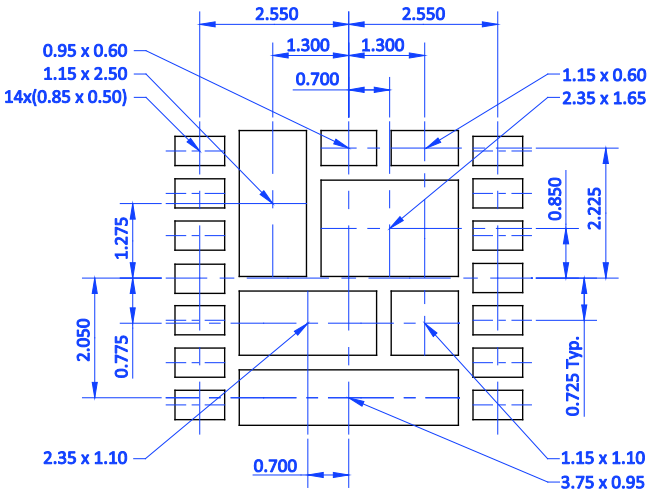
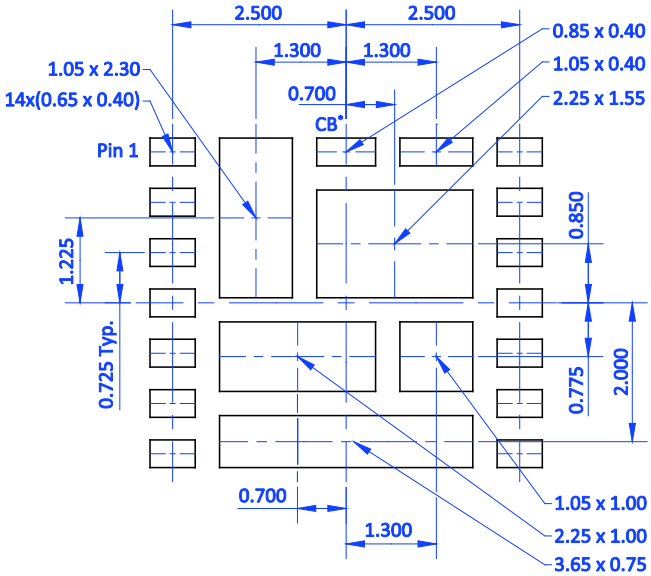


Figure 8 Solder mask



* The CB pad is usually connected to an isolated pad on the PCB. However, if extra capacitance is required, this connection may be extended and extra capacitors connected between CB and V_{SW1}.

Figure 9 Copper pads and tracks

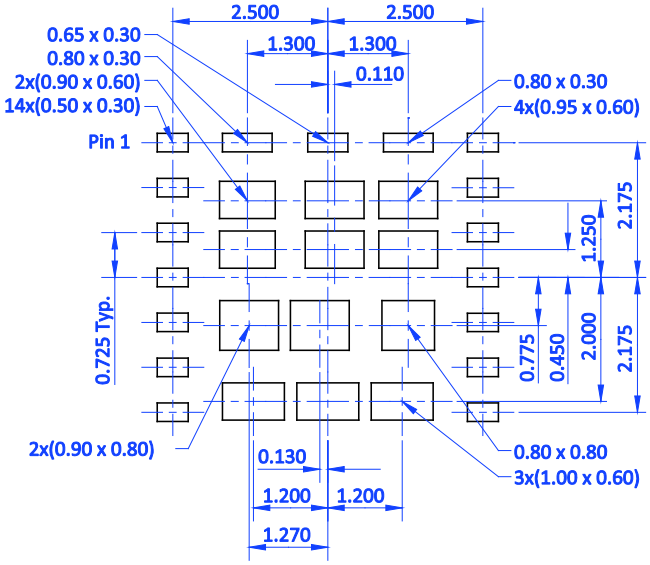


Figure 10 Solder stencil

P52F1 series

Package description

P52F1 series µPOL® products are designed for use with standard surface-mount technology (SMT) population techniques. They have a positive (raised) footprint (Figure 11), with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

The footprint design is the first of a new generation for µPOL® called Stiletto™. It has been extensively researched and delivers many benefits for products of this type and class. As a result, the package works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

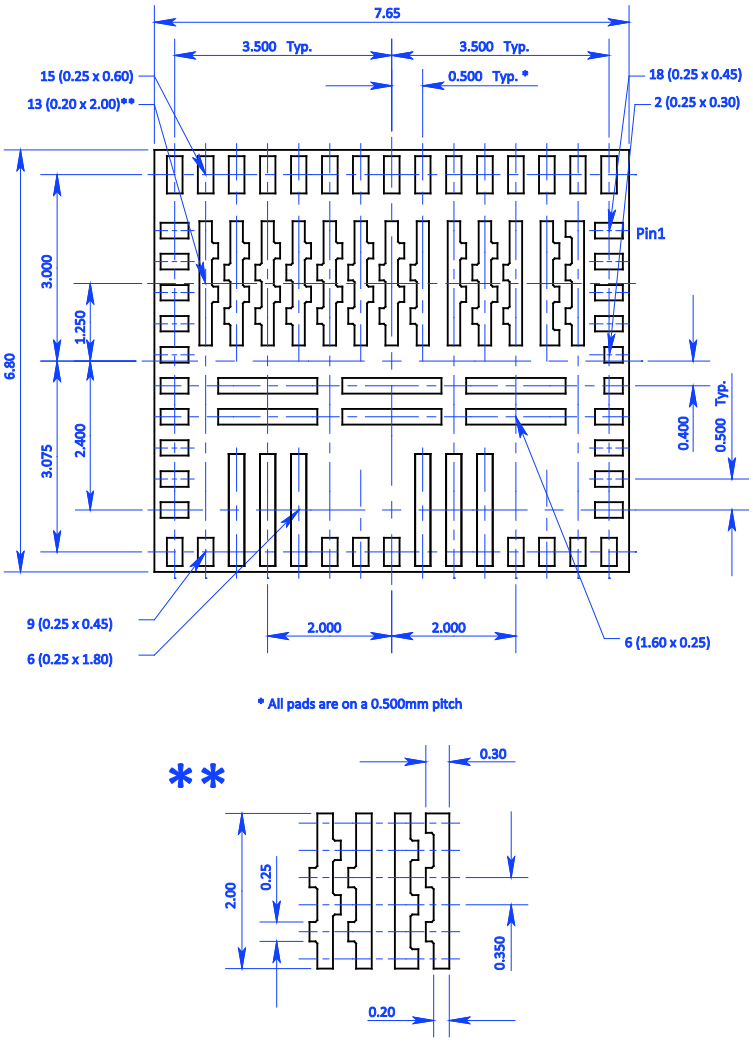


Figure 11 Package footprint (bottom view)

Board layout

Copper pads and tracks

The copper layer of the board has been biased by 25µm on each side. The copper area on the top surface should ideally be the same size or slightly larger than the device footprint.

For best results, the grouped PGnd pads and the adjacent grouped PV_{IN}* pads should be connected through to the inner layers of the PCB using filled-via technology, µVia technology or intrusive reflow technology. Using the PCB to dissipate the thermal energy from the device is extremely effective.

* Effective thermal use of PV_{IN} requires the PV_{IN} pad to be connected to one or more of the inner layers.

Note: The smaller PV_{IN} pads and PGnd pads should be connected to the grouped pads through the PCB (Figure 13). They are not connected in the package.

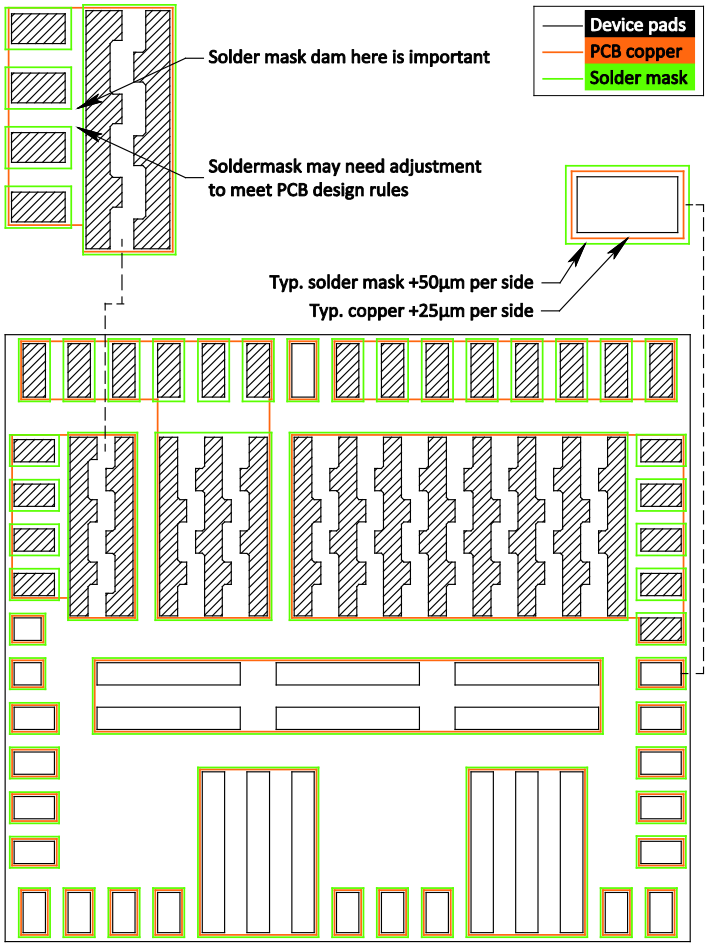


Figure 12 Copper pads and tracks

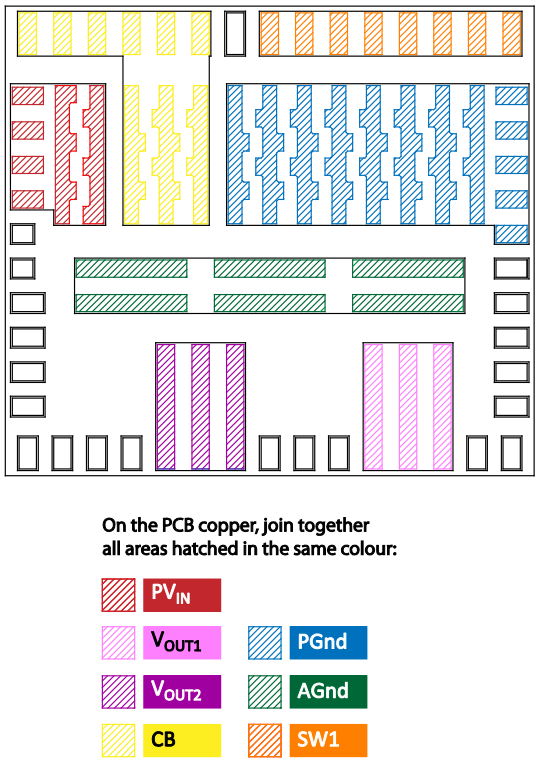


Figure 13 Pad groupings

Solder mask

The recommended design (Figure 15) uses mainly non-solder-mask-defined pads, with some exceptions. As the design has been tested with good results, deviations from it should be considered carefully. In particular, there are solder mask dams between the perimeter pads and the inner pads (Figure 12). Removing these dams can allow solder to migrate around the pads and result in some pads not being correctly soldered (Figure 14).

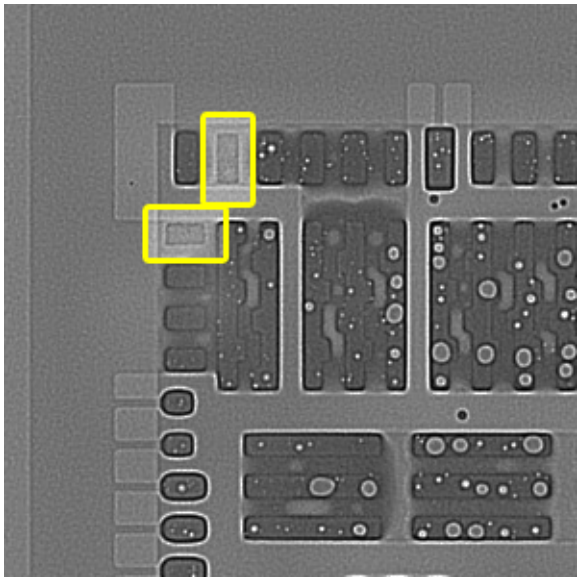


Figure 14 X-ray showing incorrectly soldered pads

Solder stencil

The design shown in Figure 16 is based on a stencil thickness of 0.100mm; it should also work adequately for a thickness of 0.125mm.

As many factors affect soldering performance, experimentation with solder volume may be required to achieve perfect results.

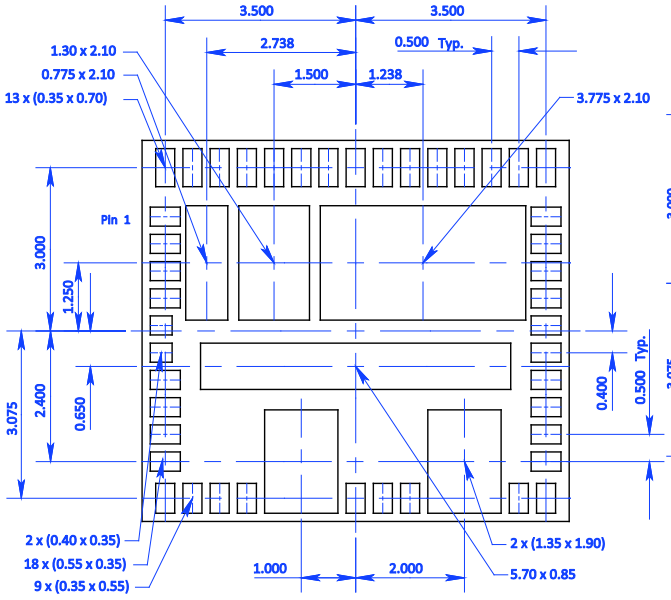


Figure 15 Solder mask

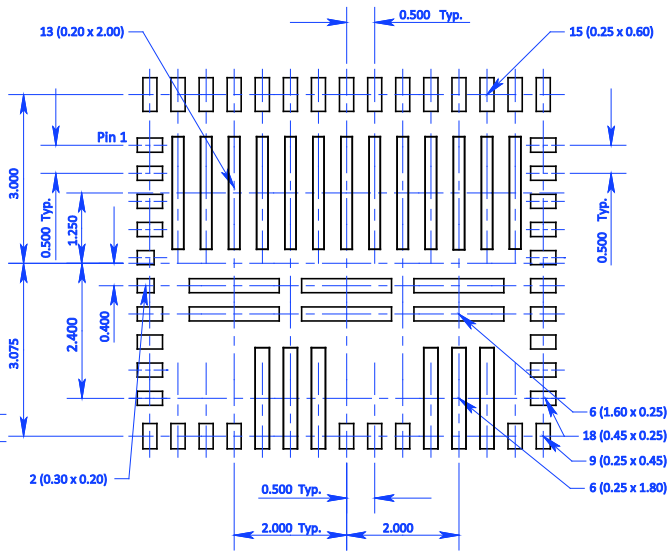


Figure 16 Solder stencil