

Equivalent Circuit Model Library

TDK Corporation Passive Application Center

July 15, 2016



< Applicable condition >

The parameters in this library are obtained under the condition of 25°C, no DC bias (excepting the DC bias model and the DC superimposition model), and small signal operation. Proper result might not be obtained if your condition is different from the above one.

< Terms and conditions regarding TDK Simulation Models >

- (1) This simulation model is being provided solely for informational purposes. Please refer to the specifications of the products in terms of detailed characteristics of such products.
- (2) In no event shall TDK Corporation of any of its subsidiaries be liable for any loss or damage arising, directly or indirectly, from any information contained in this simulation model, including, but not limited to loss or damages arising from any inaccuracies, omissions or errors in connection with such information.
- (3) Any and all copyrights on this simulation model are owned by TDK Corporation. Duplication or redistribution of this simulation model without prior written permission from TDK Corporation is prohibited.
- (4) This simulation model is subject to any modification or change without any prior notice.
- (5) Neither TDK Corporation nor any of its subsidiaries shall make any warranty, express or implied, including but not limited to the correctness, implied warranties of merchantability and fitness for a particular purpose with respect to this simulation models.
- (6) The use of this simulation model shall be deemed to have consented to the terms and conditions hereof.

< How to use with HSPICE[®] >

The files are the specific format of HSPICE.

Include the model file and add the subckt call in the circuit in which the model is used.

file name "C1005X5R0J105K050BB_b_HSPICE.mod"	file name "any_circuit.sp"
<pre>file name "C1005X5R0J105K050BB_b_HSPICE.mod" * * * SPICE Netlist Generated by TDK-EPC Corporation * Copyright(C) 2014 TDK-EPC Corporation. * All Rights Reserved. * * * * * * * * * * * * * * * * * * *</pre>	<pre>file name "any_circuit.sp" *example for using a DC bias model from TDK .include "C1005X5R0J105K050BB_b_HSPICE.mod" X1 1 2 C1005X5R0J105K050BB_b "any circuit .end</pre>
<pre>.bbbckt [1000000000000000000000000000000000000</pre>	

*HSPICE is a registered trademark of Synopsys, Inc.

< How to use with LTspice[®] >

This library includes two types of the files;*.asy files and *.mod files. Save these files at one of the following directories.

1)Save both asy and mod files at the directory where intended simulation circuit(*.asc) is saved In this case, the model can be used only in the simulation circuits saved at the same directory

🔨 any_circuit.asc	simulation circuit(*.asc)
C1005X5R1A105K050BB.asy	symbol file(*.asy)
C1005X5R1A105K050BB_b_LTspice.mod	netlist file(*.mod)

2)Save an asy file at C:/Program Files/LTC/LTspiceIV/lib/sym Save a mod file at C:/Program Files/LTC/LTspiceIV/lib/sub In this case, the model can be used in all the simulation circuits.



*LTspice is a registered trademark of Linear Technology Corporation.

< How to use with LTspice >

Perform Edit > Component, then Select Components Symbol window opens..

At Top Directory, select the directory where the asy file is saved. Then, the component will appear. Double-click the component name to place it in the schematic.



*LTspice is a registered trademark of Linear Technology Corporation.

< How to use with PSpice[®] >

This library includes two types of the files;*.olb file and *.inc file. Load these files by the following procedure.

< Loading an inc file >

Perform PSpice > Edit Simulation Profile. In the Simulation Setting window, open the Configuration Files tab. Select Include in the Category field. Click the Browse and select an inc file. Then, click either Add as Global or Add to Design.



*OrCAD, PSpice, and Capture are registered trademarks of Cadence Design Systems, Inc.



< Loading an olb file >

Open any schematic in Capture and perform Place > Part... In the Place Part window, click the Add Library icon and select an olb file. Click the part name in the Part List to place the component in the schematic.





*OrCAD, PSpice, and Capture are registered trademarks of Cadence Design Systems, Inc.



< Comparison between equivalent circuit models and measured data >

Comparison between the equivalent circuit models and measured data are shown in the following. Since the equivalent circuit models well match to measured results as shown in the following pages, simulation result that matches to actual property can be obtained.

Capacitor "C0603CH1H101J030BA"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for capacitors. Loss of actual capacitors is precisely modeled in the Loss model.

Capacitor "C1005X5R1A105K050BB"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for capacitors. Loss of actual capacitors is precisely modeled in the Loss model.

Comparison of model and measurement (3)

Inductor "MLG1005S10NJT000"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for inductors. Loss of actual inductors is precisely modeled in the precise model.

⇔⊤

Comparison of model and measurement (4)

Chip Bead "MMZ0603D800CT000"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for chip beads. Loss of actual chip beads is precisely modeled in the precise model.

欲丁

3-Terminal Filter "ACH32C-101-T001"



Comparison of model and measurement (6)

Common-Mode Filter "TCM0605G-900-2P"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for common mode filters. Property of actual common mode filter is precisely modeled in the precise model.

公TDK

Comparison of model and measurement (7)

Pulse Transformer "ALT3232M-151-T001"



Note: Two kinds of equivalent circuit models (simple model and precise model) are prepared for pulse transformers. Property of actual pulse transformer is precisely modeled in the precise model.

